

Model Name: X48-DS5 1.11

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	TABLE LIST
05	P4_LGA775_A
06	P4_LGA775_B
07	P4_LGA775_C
08	P4_LGA775_D
09	GMCH-BEARLAKE_HOST
10	GMCH-BEARLAKE_DDRII
11	GMCH-BEARLAKE_PCI E, DMI
12	GMCH-BEARLAKE_INT VGA
13	GMCH-BEARLAKE_GND
14	DDRII CHANNEL A 1,2
15	DDRII CHANNEL B 1,2
16	DDRII TERMINATION
17	PCI EXPRESS X 16 SLOT1
18	ICH9 PCI, USB, DMI, LAN
19	ICH9 GPIO, CTRL
20	ICH9 SATA, FAN PWM
21	ICH9 VCC, GND
22	CLOCK GEN ICS9LPRS914
23	PCI EXPRESS X16 SLOT 2
24	PCI SLOT 1, 2
25	PCI EXPRESS X1 SLOT 1, 2 ,3
26	ITE 8718 EX ,TPM
27	COM_LPT, -PROHOT,DYNAMIC OC

SHEET TITLE

28	DUAL BIOS
29	ALC889
30	REAR AUDIO JACK
31	VCORE PWM_ISL6327CRZ-1
32	VCORE PWM_ISL6327CRZ-2
33	VCORE PWM_ISL6327CRZ-3
34	DISCRETE POWER I
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37	REALTEK RTL8111B-1
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39	FP,FUSB,FDD
40	TI TSB43AB23 1394
41	JMB363
42	HWM,KB/MS, FAN CTRL
43	DDR POWER
44	GMCH POWER

Gigabyte Technology

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Cover Sheet			
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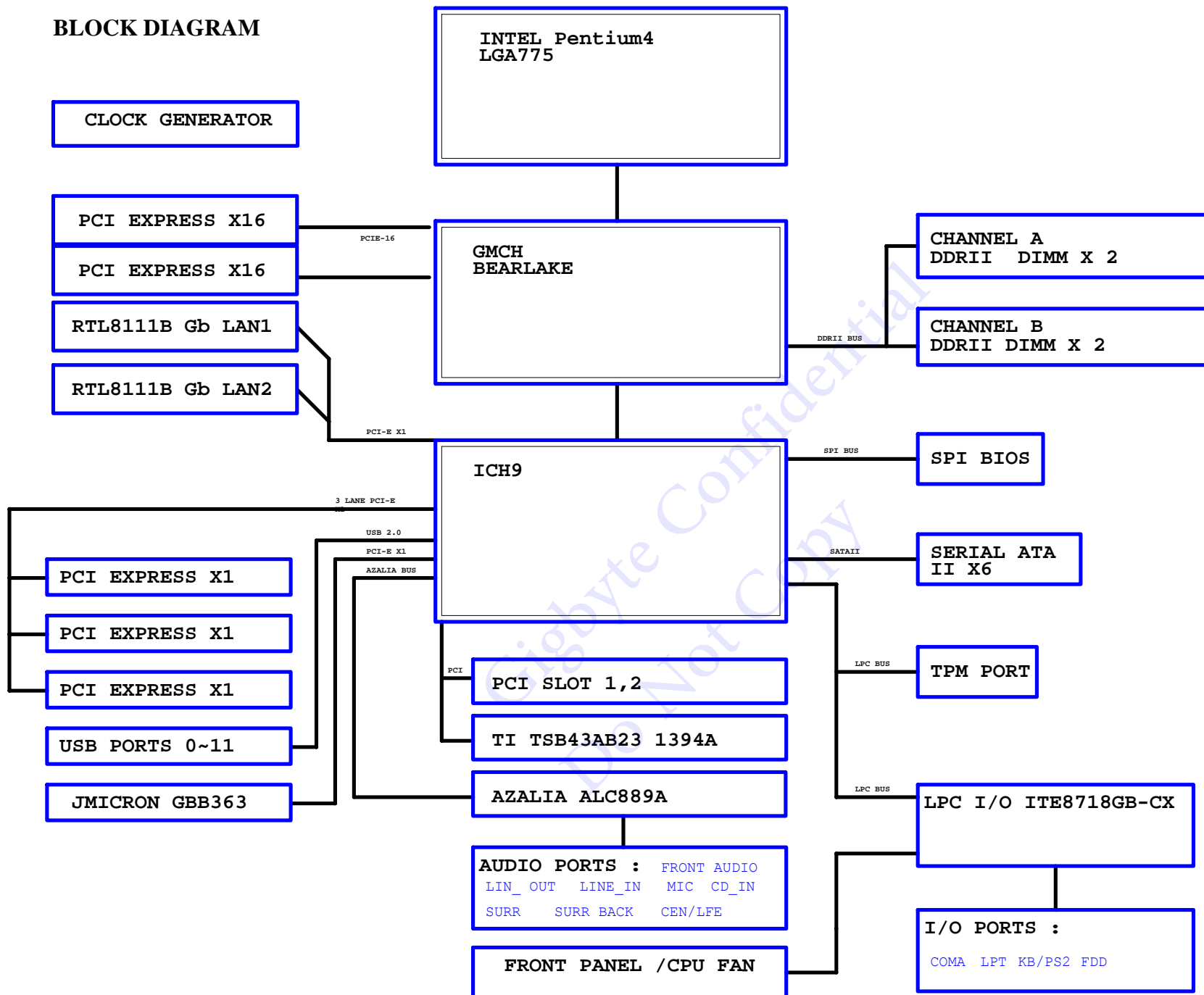
GA-X48-DS5 Version: 1.11

Circuit or PCB layout change
for next version

Component value change history

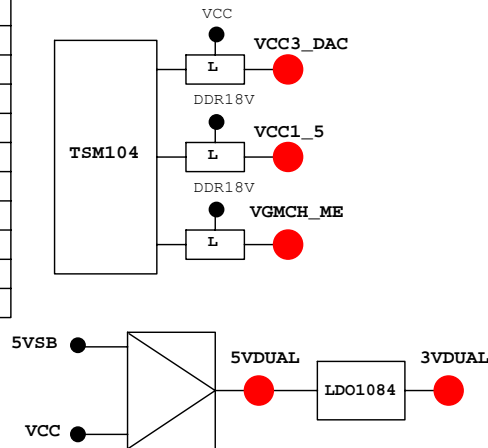
[illegible][illegible]

BLOCK DIAGRAM



LOW	5				4		3		2		1		
	ICH9 GPIO LIST TABLE												
PIN NAME		PWR WELL		AFTER/ ELTRST IN		USAGE		NOTE					
GP0		MAIN		IN		VTT_GMCH_OV3							
GP1/TACH1		MAIN		IN		ICH_FAN_TACH1		P/U 8.2K VCC3					
GP2/PIRQE#		MAIN		IN		-PIRQE		P/U 8.2K VCC3					
GP3/PIRQF#		MAIN		IN		-PIRQF		P/U 8.2K VCC3					
GP4/PIRQG#		MAIN		IN		-PIRQG		P/U 8.2K VCC3					
GP5/PIRQH#		MAIN		IN		-PIRQH		P/U 8.2K VCC3					
GP6/TACH2		MAIN		IN		ICH_FAN_TACH2		P/U 8.2K VCC3					
GP7/TACH3		MAIN		IN		ICH_FAN_TACH3		P/U 8.2K VCC3					
GP8		STBY		IN		DDR18V_OV4							
GP9		STBY		H-Z		GPIO9(DUALBIOS_INPUT)							
GP10		STBY		H-Z		DDR18V_OV5		P/D 100K GND/X					
GP11/SMBALERT#		STBY		NATIVE		-SMBALRT		P/U 8.2K 3VDUAL					
GP12		STBY		L	OUT	AUDIO_DETECT		P/U 8.2K VCC3					
GP13		STBY		L	IN	-LPCPME		P/U 8.2K 3VDUAL					
GP14		STBY		H-Z		DDR18V_OV2		P/U 8.2K 3VDUAL					
GP15		STBY		H-Z		SPI_WP		STP_PCI#					
GP16		MAIN		L	OUT	DUAL BIOS CONTROL		N/A					
GP17/TACH0		MAIN		IN		ICH_FAN_TACH0		P/U 8.2K VCC3					
GP18		MAIN		H	OUT	MB_ID1		P/U 8.2K VCC3					
GP19		MAIN		IN		VCC15_OV1		P/U 8.2K VCC3/X					
GP20		MAIN		OUT		-SPI_WP0		P/U 1K 3VCL					
GP21		MAIN		IN		VCC15_OV3		P/U 8.2K VCC3					
GP22		MAIN		IN		VCORE_OV3		P/U 8.2K VCC3					
GP23		MAIN		OUT		-LDRQ1		P/U 8.2K VCC3					
GP24		STBY		OUT		TLS		P/U 8.2K 3VDUAL					
GP25		STBY		IN		MB_ID2(STP_CPU-)		P/U 8.2K 3VDUAL					
GP26/S4_STATE#		STBY		OUT		MB_ID0		P/U 8.2K 3VDUAL					
GP27		STBY		OUT/LOW		GPIO27(EL_STATE0)		P/U 8.2K 3VDUAL					
GP28		STBY		OUT/LOW		DUAL BIOS CONTROL		N/A					
GP29/OC5#		STBY		IN		-USBOC_R		P/U FUSEVCC					
GP30/OC6#		STBY		IN		-USBOC_R		P/U FUSEVCC					
GP31/OC7#		STBY		IN		-USBOC_R		P/U FUSEVCC					
GP32		MAIN		OUT		DUAL BIOS		P/U 100K+1M VCC3					
GP33		MAIN		OUT									
GP34		MAIN		OUT/LOW				N/A					
GP35		MAIN		L	OUT	400K FS CONTROL		N/A					
GP36		MAIN		IN		DUAL BIOS CONTROL		P/U 8.2K VCC3					
GP37		MAIN		IN		150K FS CONTROL		P/U 8.2K VCC3					
GP38		MAIN		IN		VCORE_OV2		P/U 8.2K VCC3					
GP39		MAIN		IN		GPIO39		P/D 8.2K GND					
GP48		MAIN		IN		VCORE_OV1		P/U 8.2K VCC3					
GP49		MAIN		IN		STARPPING		P/D 8.2K					

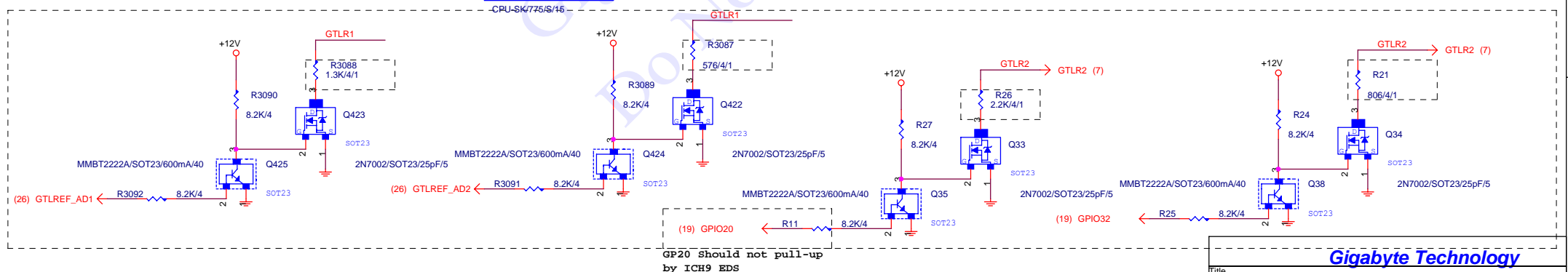
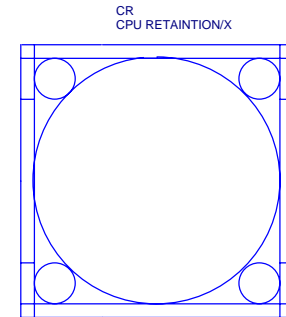
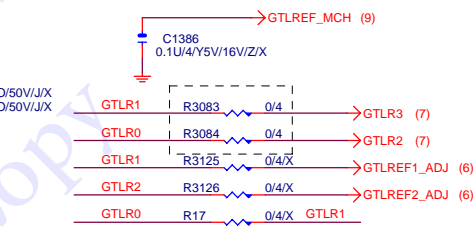
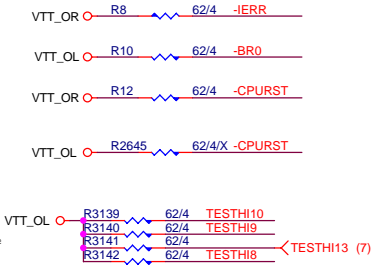
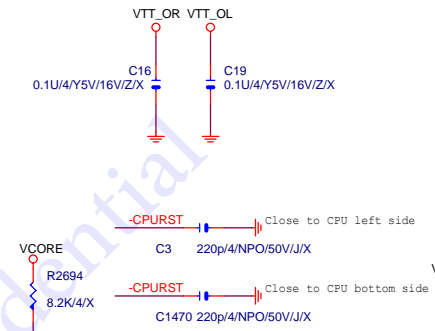
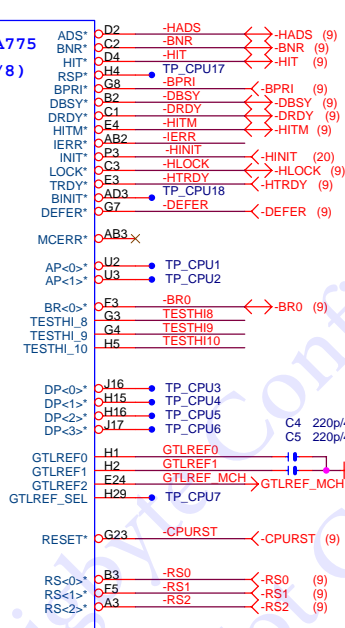
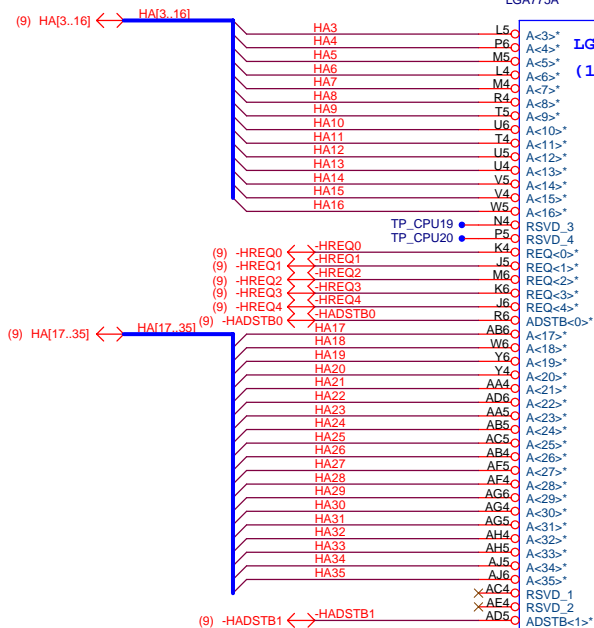
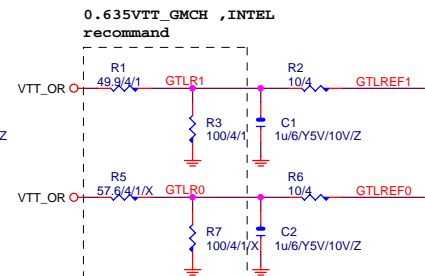
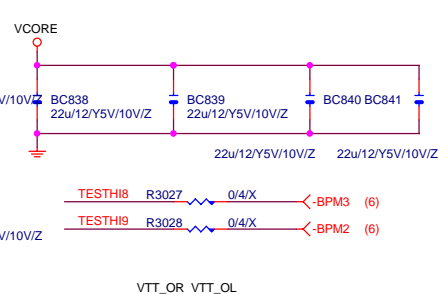
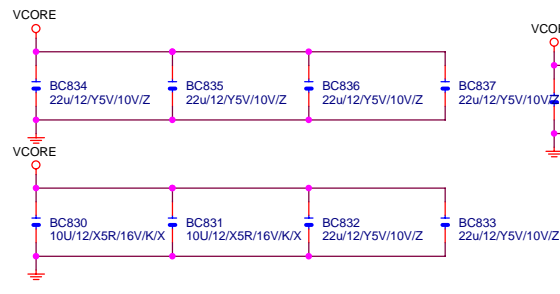
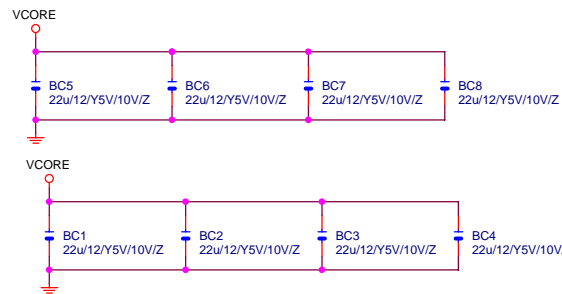
PIN NAME		PWR WELL		AFTER/ ELTRST	USAGE	NOTE				
GP50		MAIN		IN	REQ1#					
GP51		MAIN		IN	GNT1#	P/U 8.2K VCC3				
GP52		MAIN		IN	REQ2#	P/U 8.2K VCC3				
GP53		MAIN		IN	GNT2#	P/U 8.2K VCC3				
GP54		MAIN		IN	REQ3#	P/U 8.2K VCC3				
GP55		MAIN		IN	GNT3#	P/U 8.2K VCC3				
GP56		STBY		IN	VCORE_OV5					
GP57		STBY		IN	VCORE_OV4					
GP58		STBY		IN	SPI_CS1#					
GP59		STBY			-USBOC_R					
GP60		STBY			LINKALRT#					



	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8718
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	ICH8
SYS FAN	FANPWM2	N/A	FANIO2	IT8718
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	ICH8
PWR FAN	N/A	N/A	FANIO3	IT8718
			ICH_FAN_TACH2	ICH8

VCORE_OV5

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TABLE LIST			
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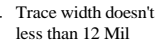


For Q-core CPU support

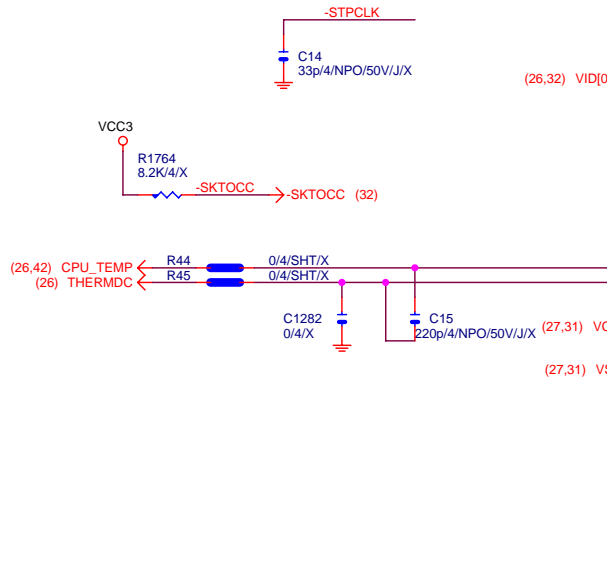
GP20 should not pull-up by ICH9 EDS

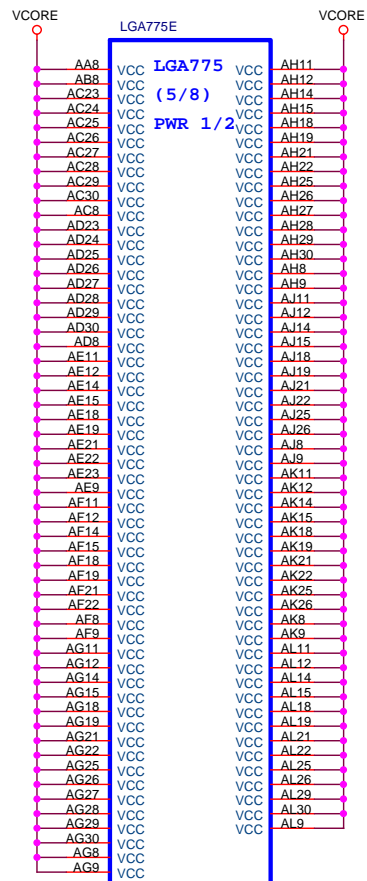
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P4_LGA775-A		
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VCCA & VCOREPLL
define doesn't same as
old P4 design kit

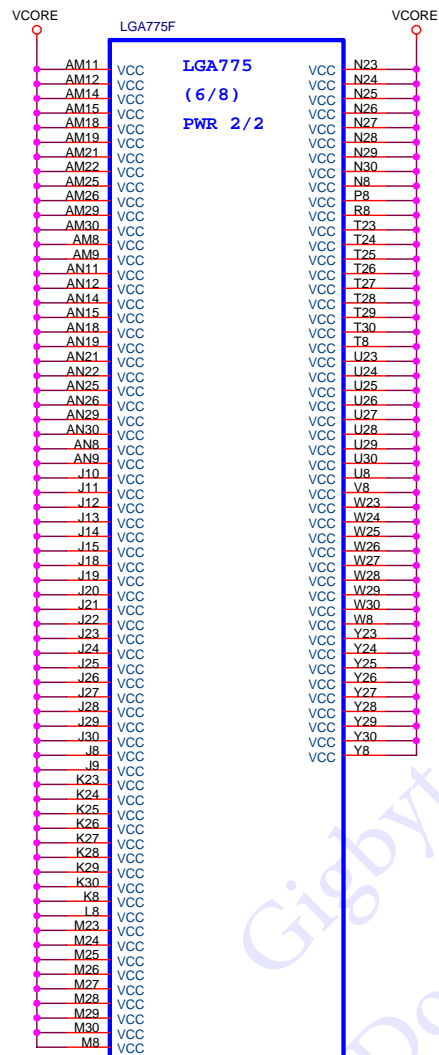


Pin-to-pin connection diagram for LGA775 to CPU-SK/775/S15. The diagram shows connections for various pins including -SMI, -A20M, -FERR, INTR, NMI, -IGNNE, -STPCLK, VCCA, VSSA, VCOREPLL, VCC_PLL, VIDO, VID1, VID2, VID3, VID4, VID5, VID6, VID7, VRD_SEL, CPUCLK, -CPUCLK, -SKTOCC, THERMDA_C, THERMDC_C, -SENSE, -SENSE, VCORE, TP_CPU11, TP_CPU14, PECL, TP_CPU16, SMI, A20M, FERR/PBE, LINT0, LINT1, IGNNE, STPCLK, VCCA, VSSA, VCOREPLL, VCC_PLL, VID<0>, VID<1>, VID<2>, VID<3>, VID<4>, VID<5>, VID<6>, VID<7>, VID_SELECT, BCLK<0>, BCLK<1>, SKTOCC, THERMDA, THERMDC, THERMDA_2, THERMDC_2, VCC_SENSE, VSS_SENSE, VCC_MB_REGULATION, VSS_MB_REGULATION, VCC_D_SENSE, MSID<0>, MSID<1>, MSID<2>, VTT_PKGSENSE, 260_50, SLEW_CTRL, SST_LV, MFG_NOBOOT, TESTHI_0, TESTHI_1, TESTHI_2, TESTHI_3, TESTHI_4, TESTHI_5, TESTHI_6, TESTHI_7, TESTHI_11, TESTHI_12, TESTHI_13, FORCEPR, CPUPWROK, -PROCHOT, -THERMTRIP, COMP<0>, COMP<1>, COMP<2>, COMP<3>, COMP<4>, COMP<5>, COMP<6>, COMP<7>, COMP<8>, TESTHI_M, R666, CPU10, GTLREF3, GTLREF2, AH2, MSID1_R53, MSID0_R55, TP_CPU12, TP_CPU13, TP_CPU15.

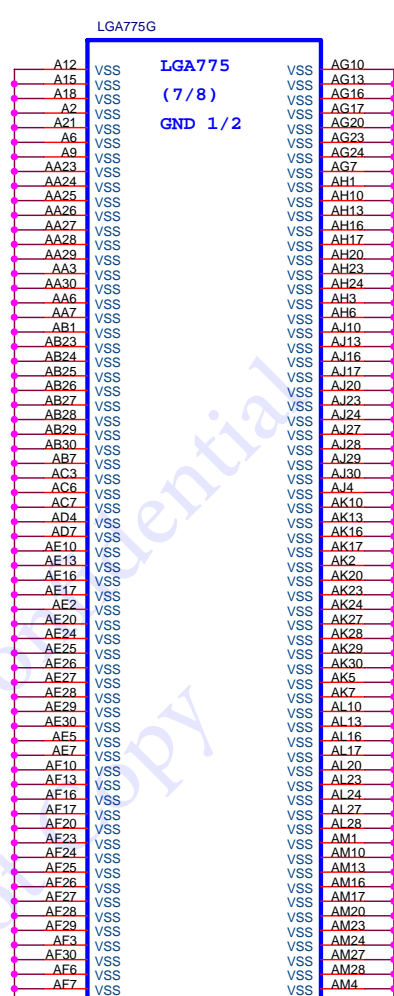
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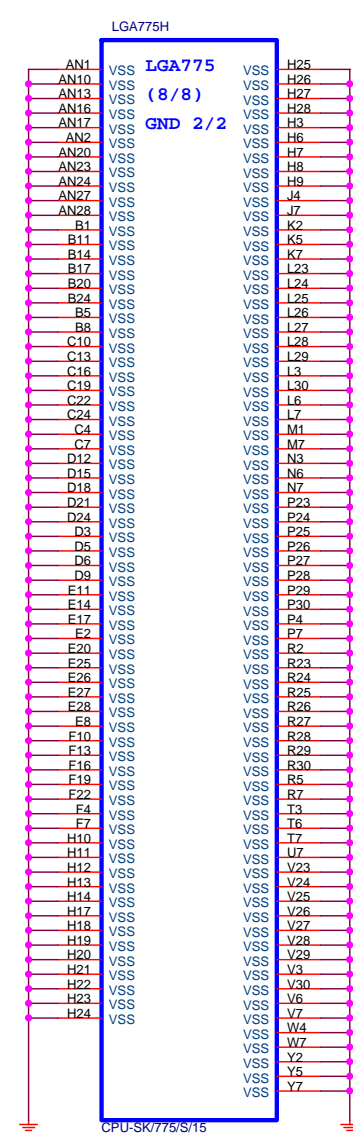
CPU-SK/775/S/15



CPU-SK/775/S/15



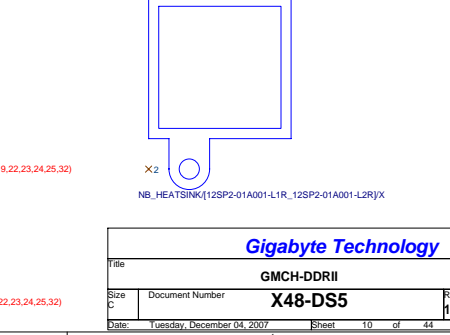
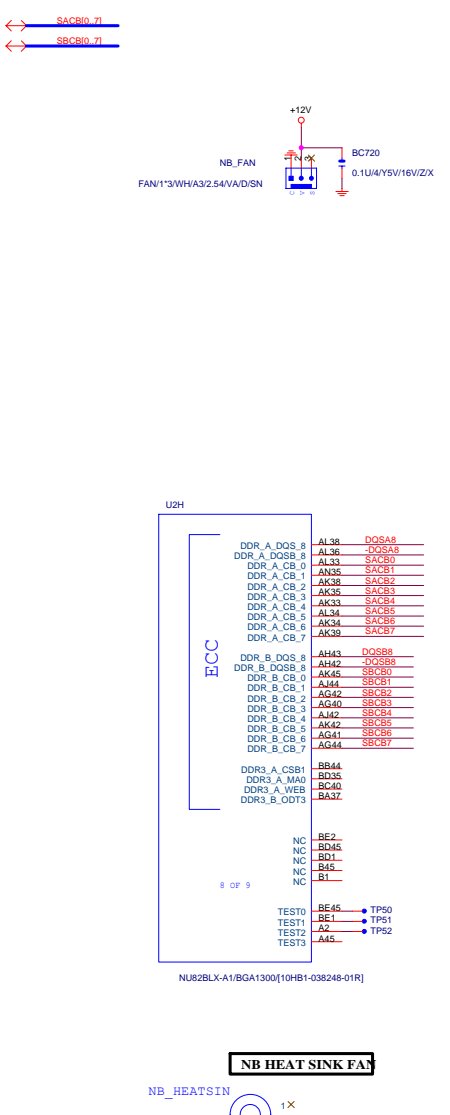
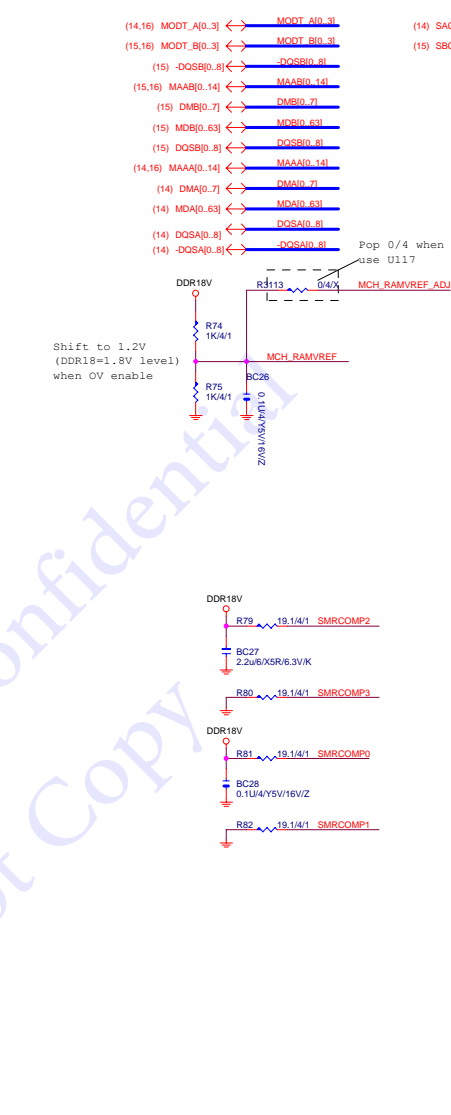
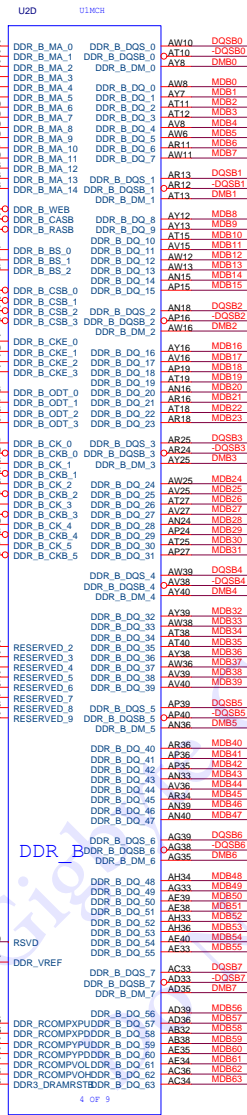
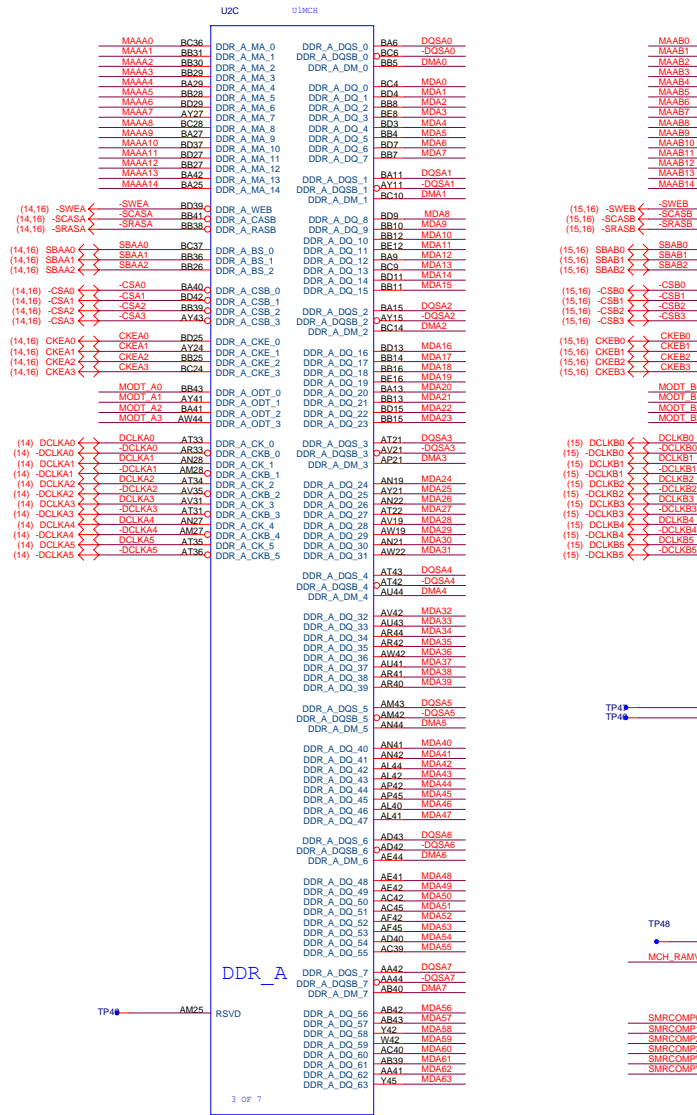
CPU-SK/775/S/15



CPU-SK/775/S/15

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VCC1_25PCIE< VCC1_25PCIE< (13)
R88
24.9/6/1
GRCOMP

EXP A TXP[0..15] >> EXP_A_TXP[0..15] (17)
EXP A TXN[0..15] >> EXP_A_TXN[0..15] (17)
EXP A RXP[0..15] >> EXP_A_RXP[0..15] (17)
EXP A RXN[0..15] >> EXP_A_RXN[0..15] (17)

VCCR_REG < VCCR_REG (13)
R3149
24.9/6/1
GRCOMP2

EXP B TXP[0..15] >> EXP_B_TXP[0..15] (23)
EXP B TXN[0..15] >> EXP_B_TXN[0..15] (23)
EXP B RXP[0..15] >> EXP_B_RXP[0..15] (23)
EXP B RXN[0..15] >> EXP_B_RXN[0..15] (23)

U2A

U1MCH

EXP A RXP0 A16 PEG_RXP_0
EXP A RXN0 B15 PEG_RXN_0
EXP A RXP1 B13 PEG_RXP_1
EXP A RXN1 C14 PEG_RXN_1
EXP A RXP2 G13 PEG_RXP_2
EXP A RXN2 G13 PEG_RXN_2
EXP A RXP3 L13 PEG_RXP_3
EXP A RXN3 K13 PEG_RXN_3
EXP A RXP4 N13 PEG_RXP_4
EXP A RXN4 M13 PEG_RXN_4
EXP A RXP5 H12 PEG_RXP_5
EXP A RXN5 G12 PEG_RXN_5
EXP A RXP6 K11 PEG_RXP_6
EXP A RXN6 L12 PEG_RXN_6
EXP A RXP7 G10 PEG_RXP_7
EXP A RXN7 H10 PEG_RXN_7
EXP A RXP8 E6 PEG_RXP_8
EXP A RXN8 D5 PEG_RXN_8
EXP A RXP9 F7 PEG_RXP_9
EXP A RXN9 G6 PEG_RXN_9
EXP A RXP10 D2 PEG_RXP_10
EXP A RXN10 C2 PEG_RXN_10
EXP A RXP11 K7 PEG_RXP_11
EXP A RXN11 K8 PEG_RXN_11
EXP A RXP12 M11 PEG_RXP_12
EXP A RXN12 L10 PEG_RXN_12
EXP A RXP13 M7 PEG_RXP_13
EXP A RXN13 M8 PEG_RXN_13
EXP A RXP14 K3 PEG_RXP_14
EXP A RXN14 J2 PEG_RXN_14
EXP A RXP15 N8 PEG_RXP_15
EXP A RXN15 N10 PEG_RXN_15

(18) DMI_0RXP >> DMI_0RXP
(18) DMI_0RXN >> DMI_0RXN
(18) DMI_1RXP >> DMI_1RXP
(18) DMI_1RXN >> DMI_1RXN
(18) DMI_2RXP >> DMI_2RXP
(18) DMI_2RXN >> DMI_2RXN
(18) DMI_3RXP >> DMI_3RXP
(18) DMI_3RXN >> DMI_3RXN

DMI_RXP_0 N5
DMI_RXN_0 M4
DMI_RXP_1 T7
DMI_RXN_1 T8
DMI_RXP_2 P4
DMI_RXN_2 R5
DMI_RXP_3 V7
DMI_RXN_3 V6

EXP_CLKINP
EXP_CLKINN
RSVD_G15
RSVD_H15

NU82BLX-A1/BGA1300/[10HB1-038248-01R]

PEG_TXP_0 D16
PEG_TXN_0 E17
PEG_TXP_1 E15
PEG_TXN_1 D14
PEG_TXP_2 E13
PEG_TXN_2 B11
PEG_TXP_3 A12
PEG_TXN_3 D10
PEG_TXP_4 E11
PEG_TXN_4 B9
PEG_TXP_5 C10
PEG_TXN_5 D8
PEG_TXP_6 E9
PEG_TXN_6 B7
PEG_TXP_7 A8
PEG_TXN_7 C6
PEG_TXP_8 B3
PEG_TXN_8 C4
PEG_TXP_9 B4
PEG_TXN_9 E3
PEG_TXP_10 D3
PEG_TXN_10 F5
PEG_TXP_11 E4
PEG_TXN_11 H1
PEG_TXP_12 G2
PEG_TXN_12 J5
PEG_TXP_13 H4
PEG_TXN_13 L5
PEG_TXP_14 K4
PEG_TXN_14 M1
PEG_TXP_15 L2
PEG_TXN_15

DMI_0TXP R7
DMI_0TXN R6
DMI_1TXP N2
DMI_1TXN P3
DMI_2TXP R2
DMI_2TXN T1
DMI_3TXP V10
DMI_3TXN V11

T10 GRCOMP
R10

EXP_COMPO
EXP_COMPI

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U2I

PCIE 2

EXP B RXP0 W12 PEG2_RXP_0
EXP B RXN0 AA13 PEG2_RXN_0
EXP B RXP1 AA10 PEG2_RXP_1
EXP B RXN1 AA11 PEG2_RXN_1
EXP B RXP2 AA6 PEG2_RXP_2
EXP B RXN2 AA7 PEG2_RXN_2
EXP B RXP3 AC13 PEG2_RXP_3
EXP B RXN3 AB12 PEG2_RXN_3
EXP B RXP4 AC11 PEG2_RXP_4
EXP B RXN4 AC10 PEG2_RXN_4
EXP B RXP5 AC6 PEG2_RXP_5
EXP B RXN5 AC7 PEG2_RXN_5
EXP B RXP6 AE13 PEG2_RXP_6
EXP B RXN6 AD12 PEG2_RXN_6
EXP B RXP7 AE10 PEG2_RXP_7
EXP B RXN7 AE11 PEG2_RXN_7
EXP B RXP8 AE7 PEG2_RXP_8
EXP B RXN8 AE6 PEG2_RXN_8
EXP B RXP9 AG12 PEG2_RXP_9
EXP B RXN9 AH13 PEG2_RXN_9
EXP B RXP10 AH11 PEG2_RXP_10
EXP B RXN10 AH10 PEG2_RXN_10
EXP B RXP11 AH7 PEG2_RXP_11
EXP B RXN11 AH6 PEG2_RXN_11
EXP B RXP12 AK12 PEG2_RXP_12
EXP B RXN12 AK13 PEG2_RXN_12
EXP B RXP13 AL11 PEG2_RXP_13
EXP B RXN13 AL10 PEG2_RXN_13
EXP B RXP14 AL6 PEG2_RXP_14
EXP B RXN14 AL7 PEG2_RXN_14
EXP B RXP15 AP10 PEG2_RXP_15
EXP B RXN15 AP11 PEG2_RXN_15

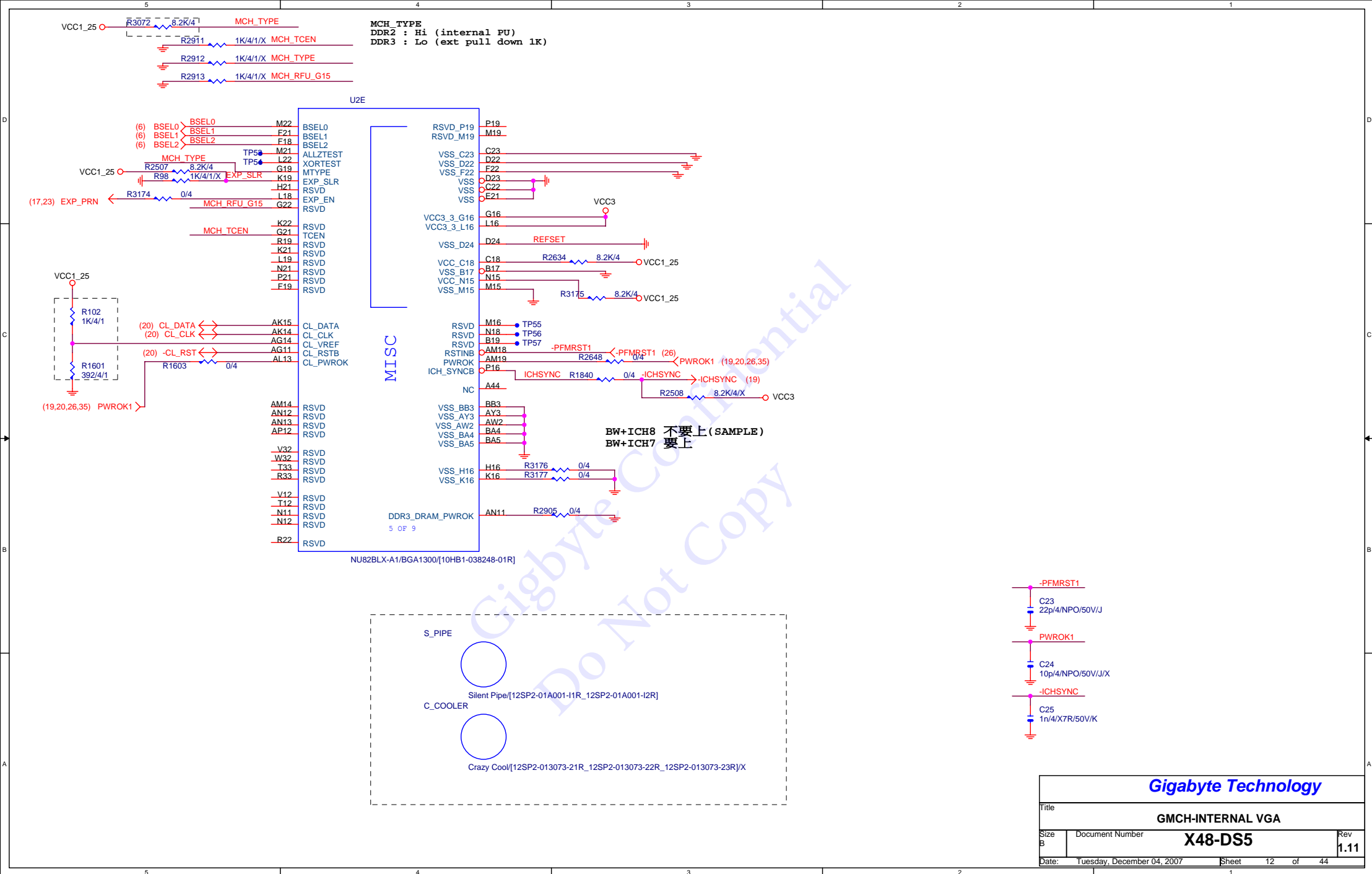
(22) -SRCCLK_MCH1 >> AD14
(22) SRCCLK_MCH1 >> AE14

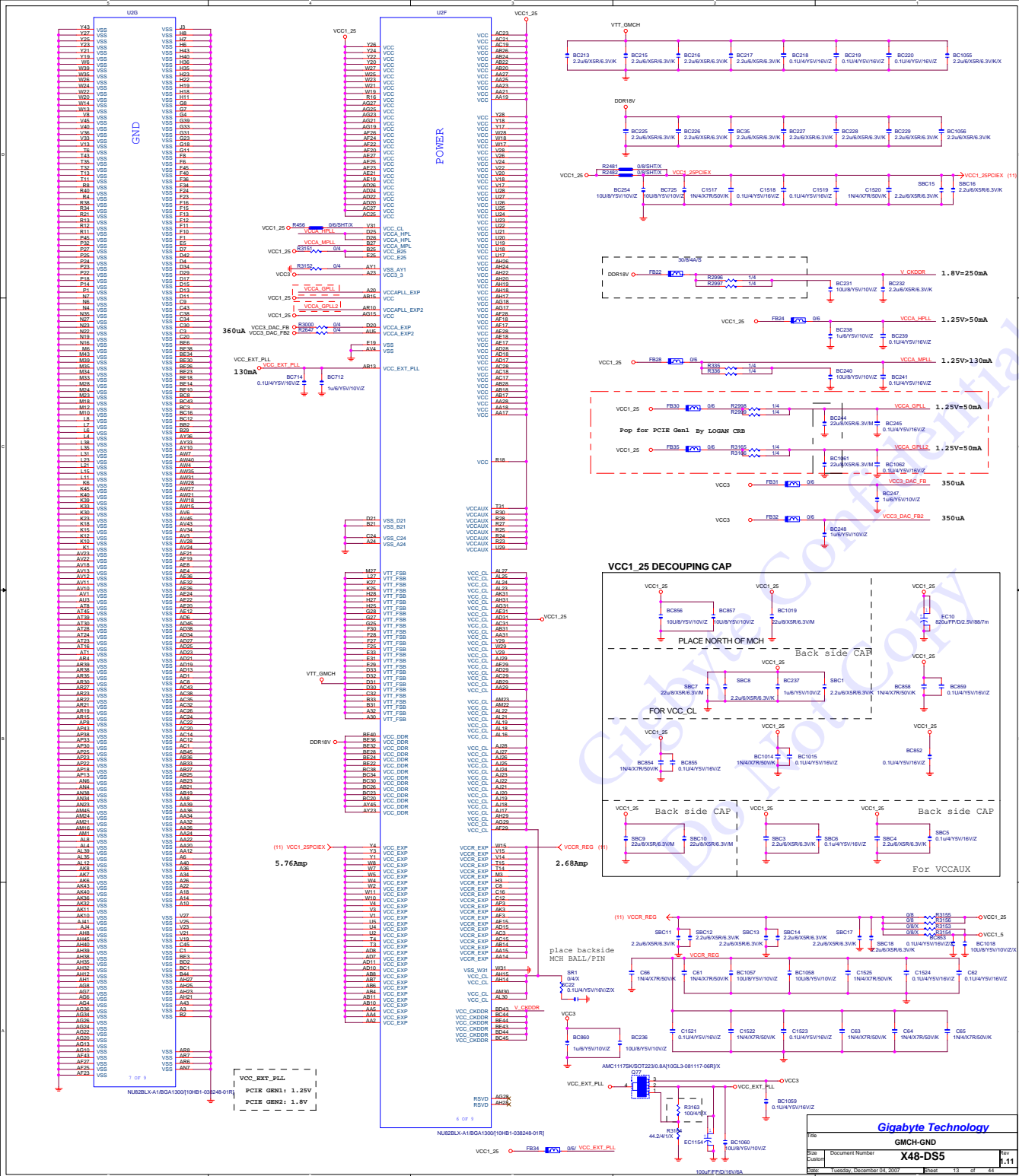
EXP2_CLKINN
EXP2_CLKINP
EXP2_COMPI
EXP2_COMPO

NU82BLX-A1/BGA1300/[10HB1-038248-01R]

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Title			
GMCH-PCI E & DMI			
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GPIO27	GPIO9	VOLTAGE
GPO/Low	GPI	Default
GPI	GPI	+10%
GPO/Low	GPO/Low	-10%

ICH

(10) CHA_ADJ ← R333 → 0.1u/4V5V/16V/Z

VREF_DDRA R1611 1K/41

BC111 0.1u/4V5V/16V/Z

R104 1K/41

0.1u/4V5V/16V/Z

0.1u/4V5V/16V/Z

0.1u/4V5V/16V/Z

0.1u/4V5V/16V/Z

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0.1u/4V5V/16V/Z

0.1u/4V5V/16V/Z

0.1u/4V5V/16V/Z

0.1u/4V5V/16V/Z

0.1u/4V5V/16V/Z

0.1u/4V5V/16V/Z

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0.1u/4V5V/16V/Z

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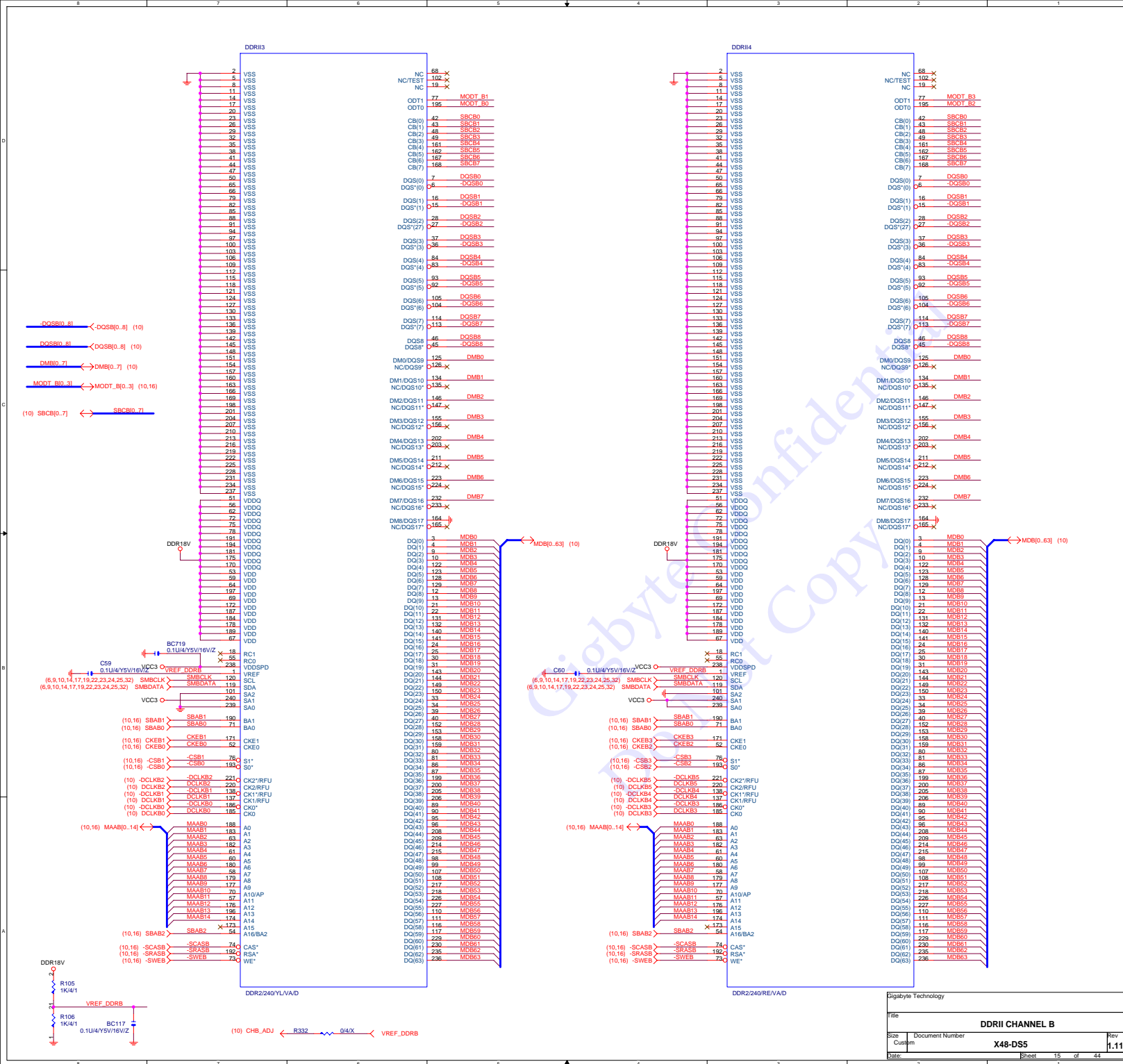
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DDR2 CHANNEL A

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Document Number
X48-DS5

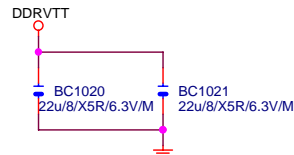
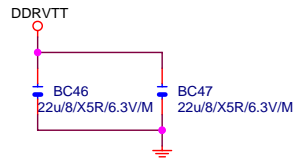
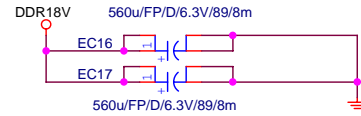
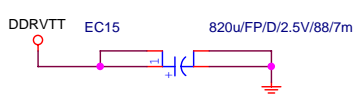
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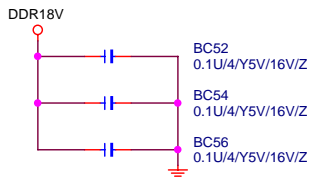


DDR TERMINATION CHANNEL A

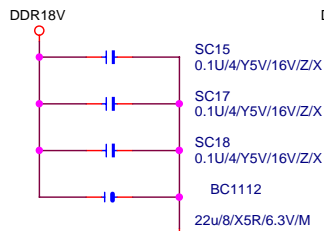
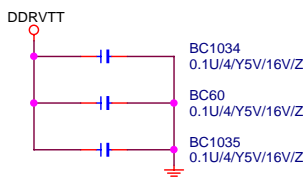
DDRVTT Decouple



DDR18V Decouple



DDRVTT Decouple



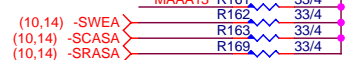
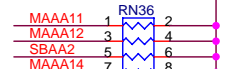
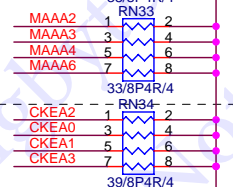
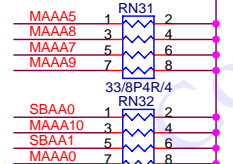
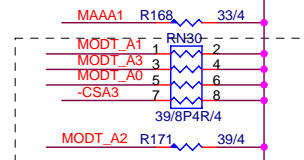
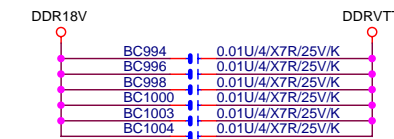
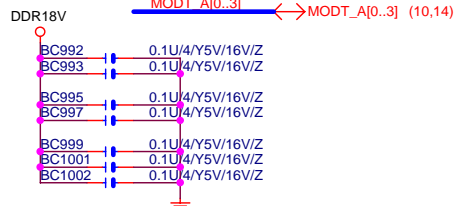
SBAAI[0..2] <- SBAI[0..2] (10,14)

CSAI[0..3] <- CSAI[0..3] (10,14)

CKEAI[0..3] <- CKEAI[0..3] (10,14)

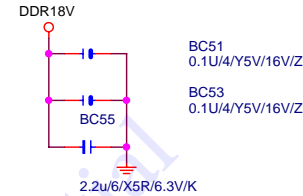
MAAAI[0..14] <- MAAAI[0..14] (10,14)

MODT_A[0..3] <-> MODT_A[0..3] (10,14)

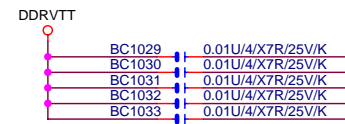
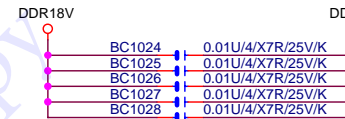
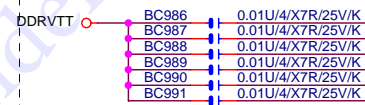
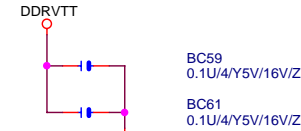


DDR TERMINATION CHANNEL B

DDR18V Decouple



DDRVTT Decouple



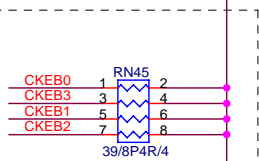
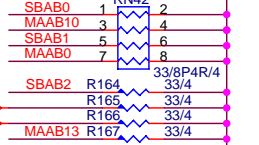
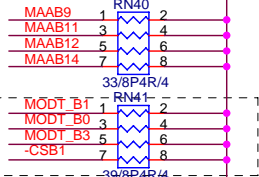
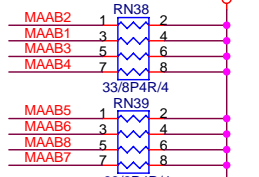
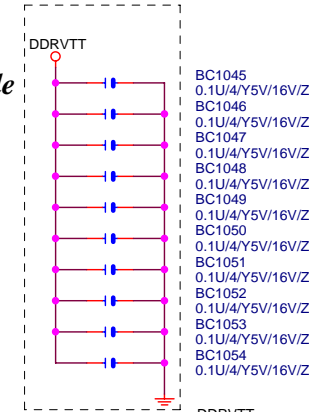
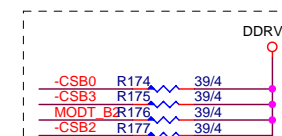
MODT_BI[0..3] <-> MODT_BI[0..3] (10,15)

SBAB[0..2] <- SBAB[0..2] (10,15)

-CSBI[0..3] <- -CSBI[0..3] (10,15)

CKEBI[0..3] <- CKEBI[0..3] (10,15)

MAABI[0..14] <-> MAABI[0..14] (10,15)

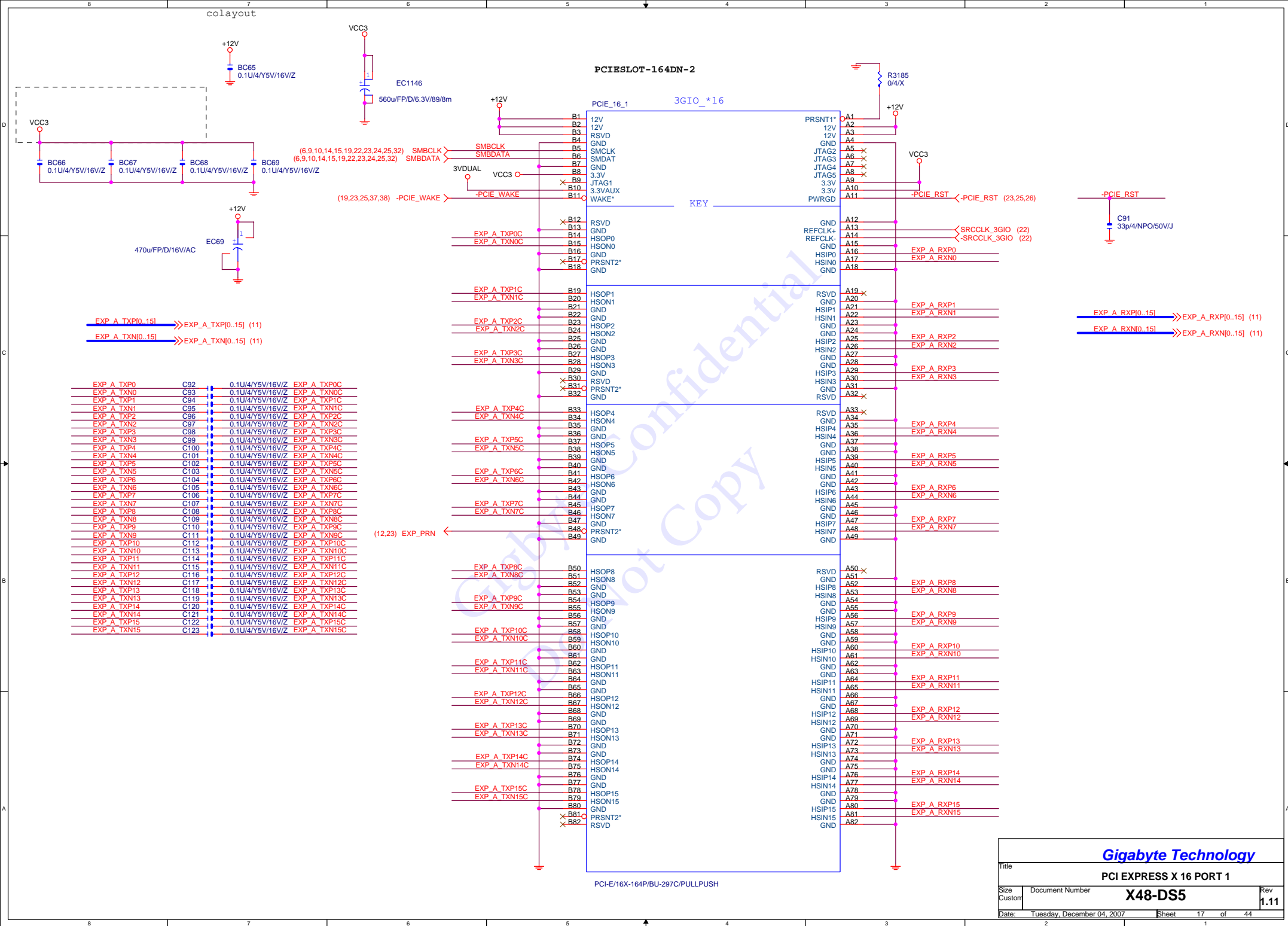


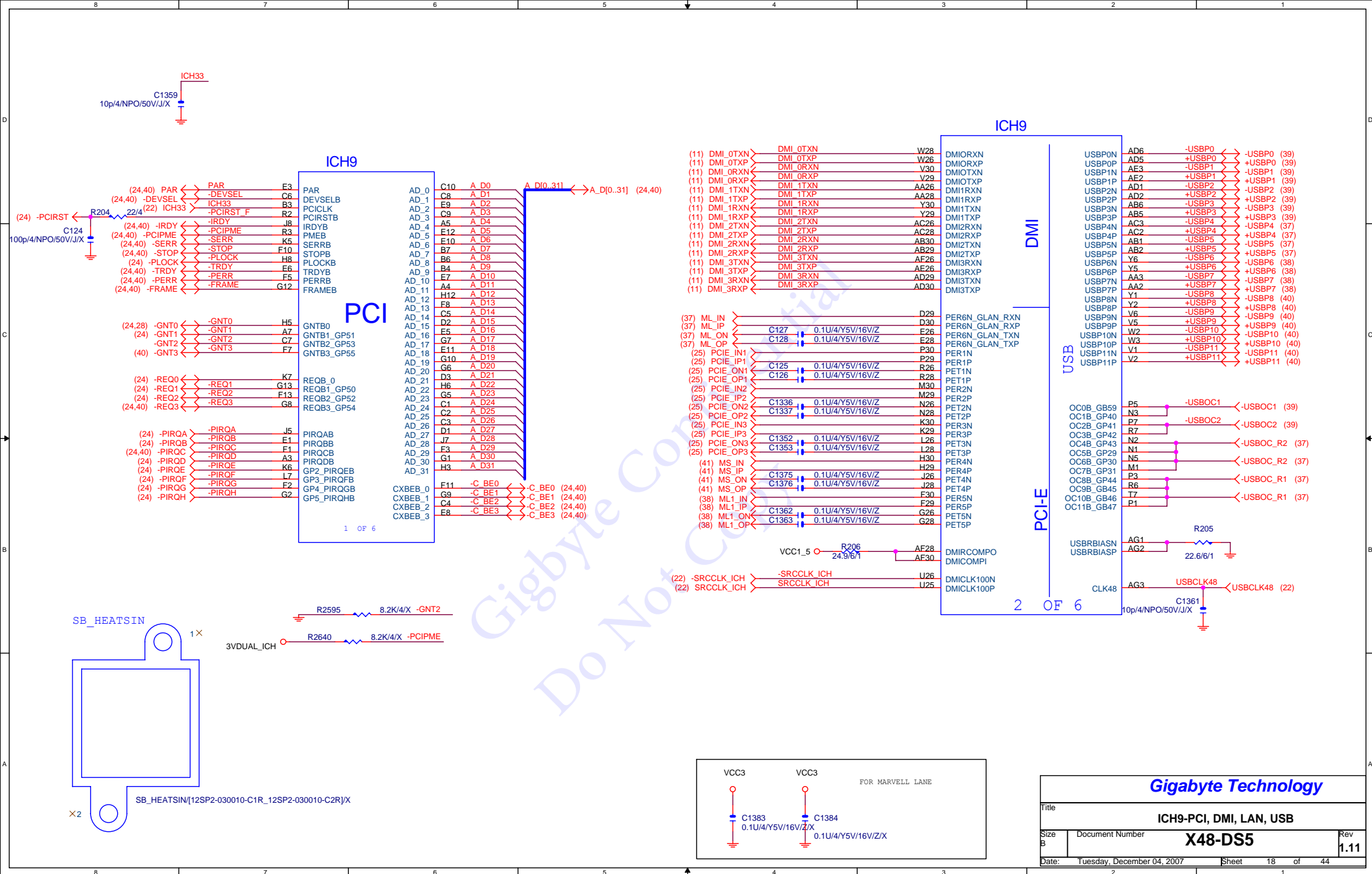
(10,15) -SCASB <-> (10,15) -SCASB

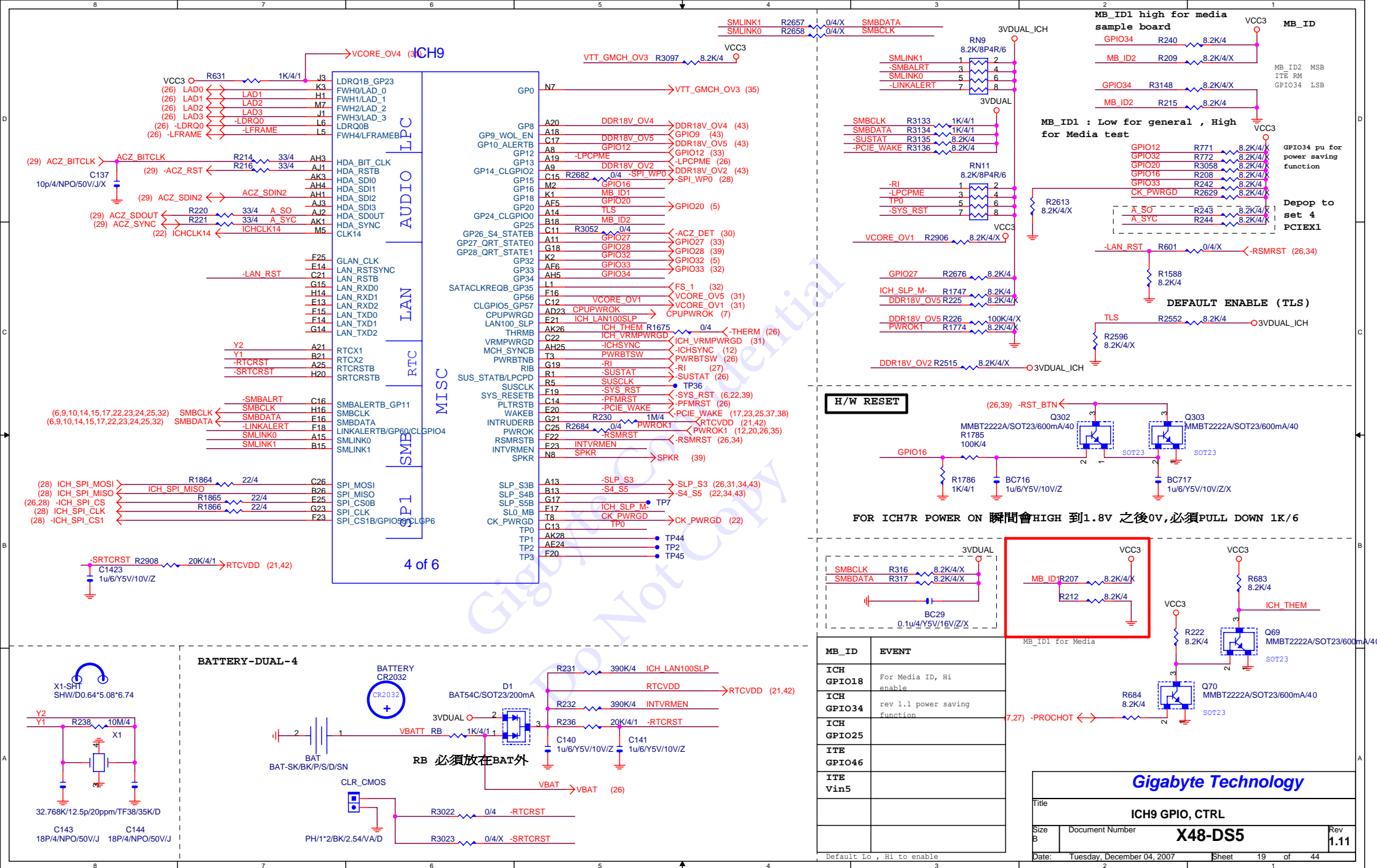
Gigabyte Technology

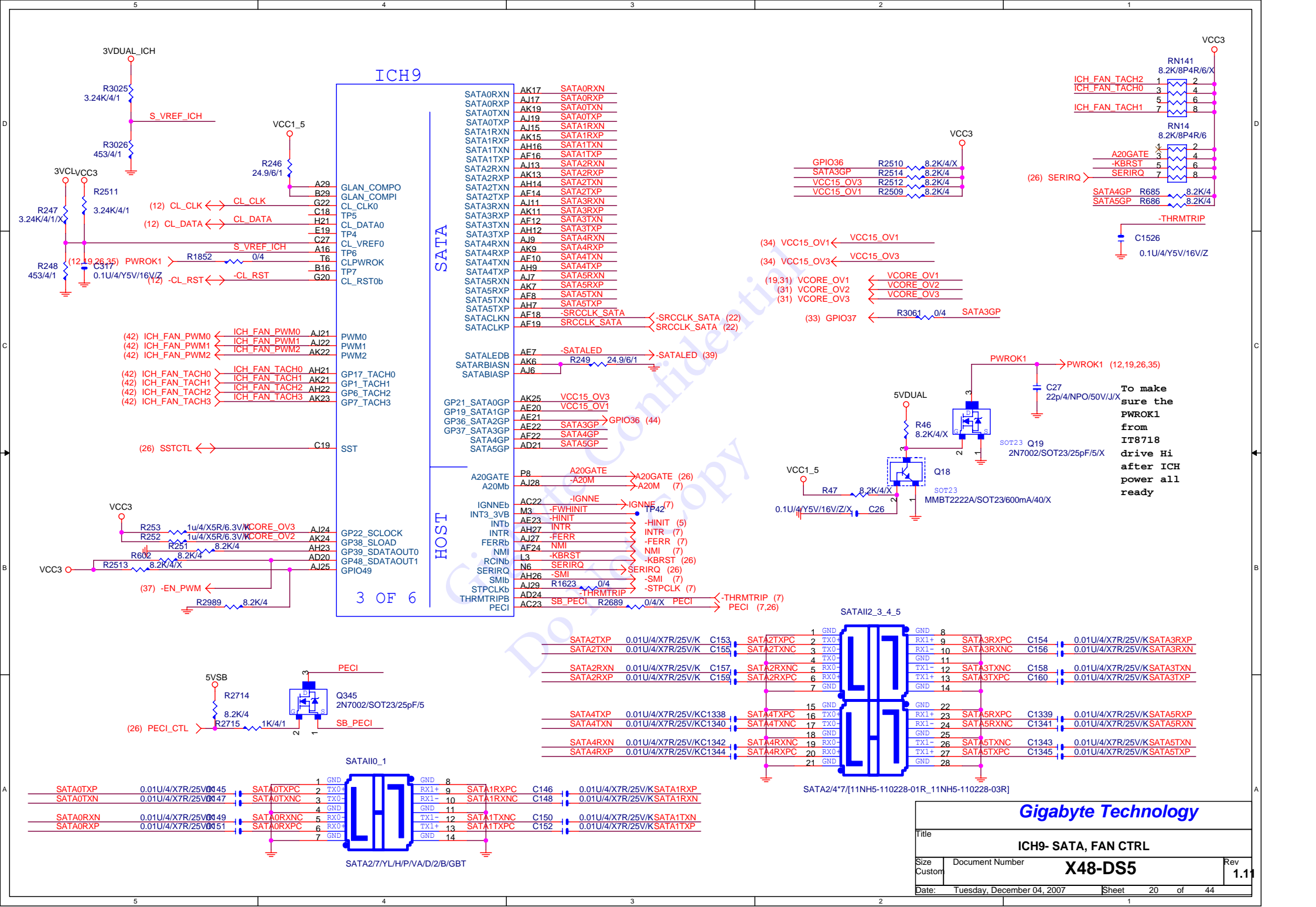
DDRII TERMINATOR

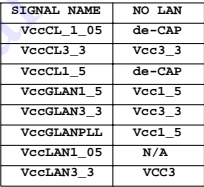
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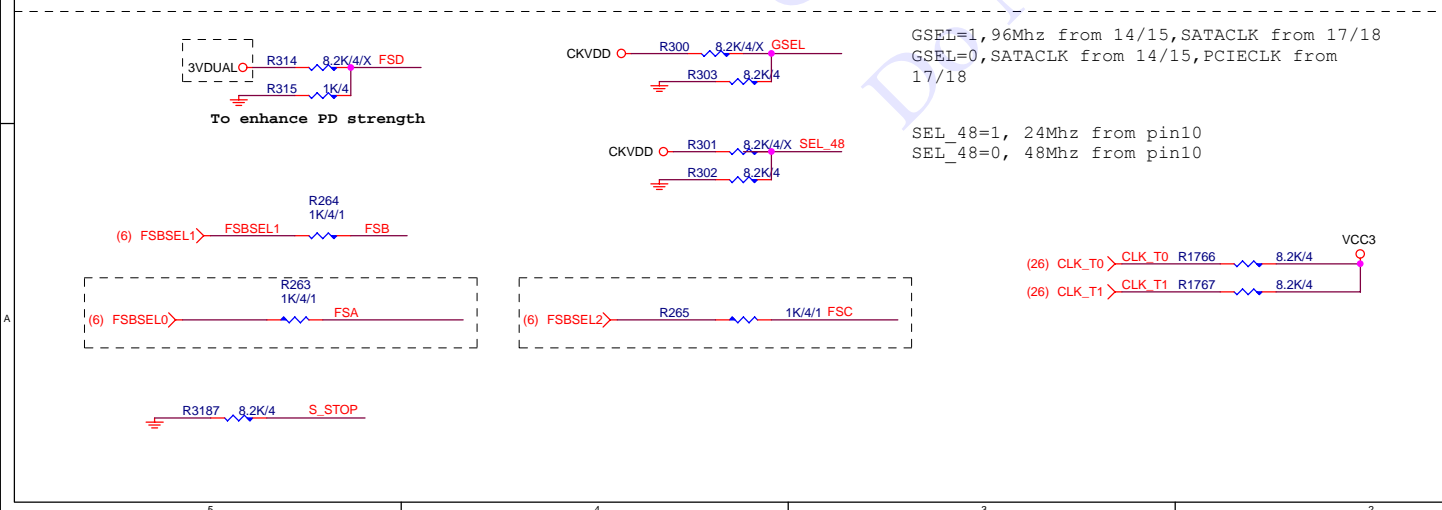
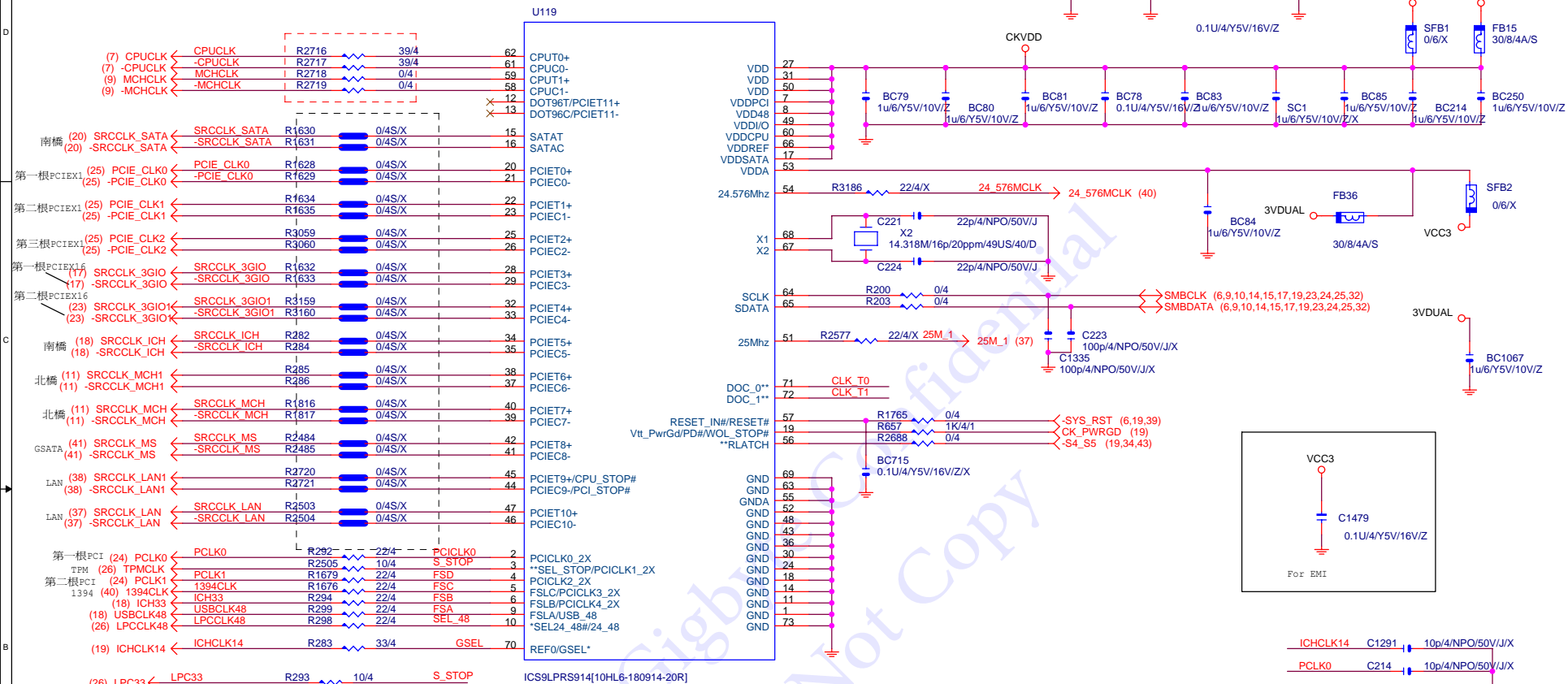






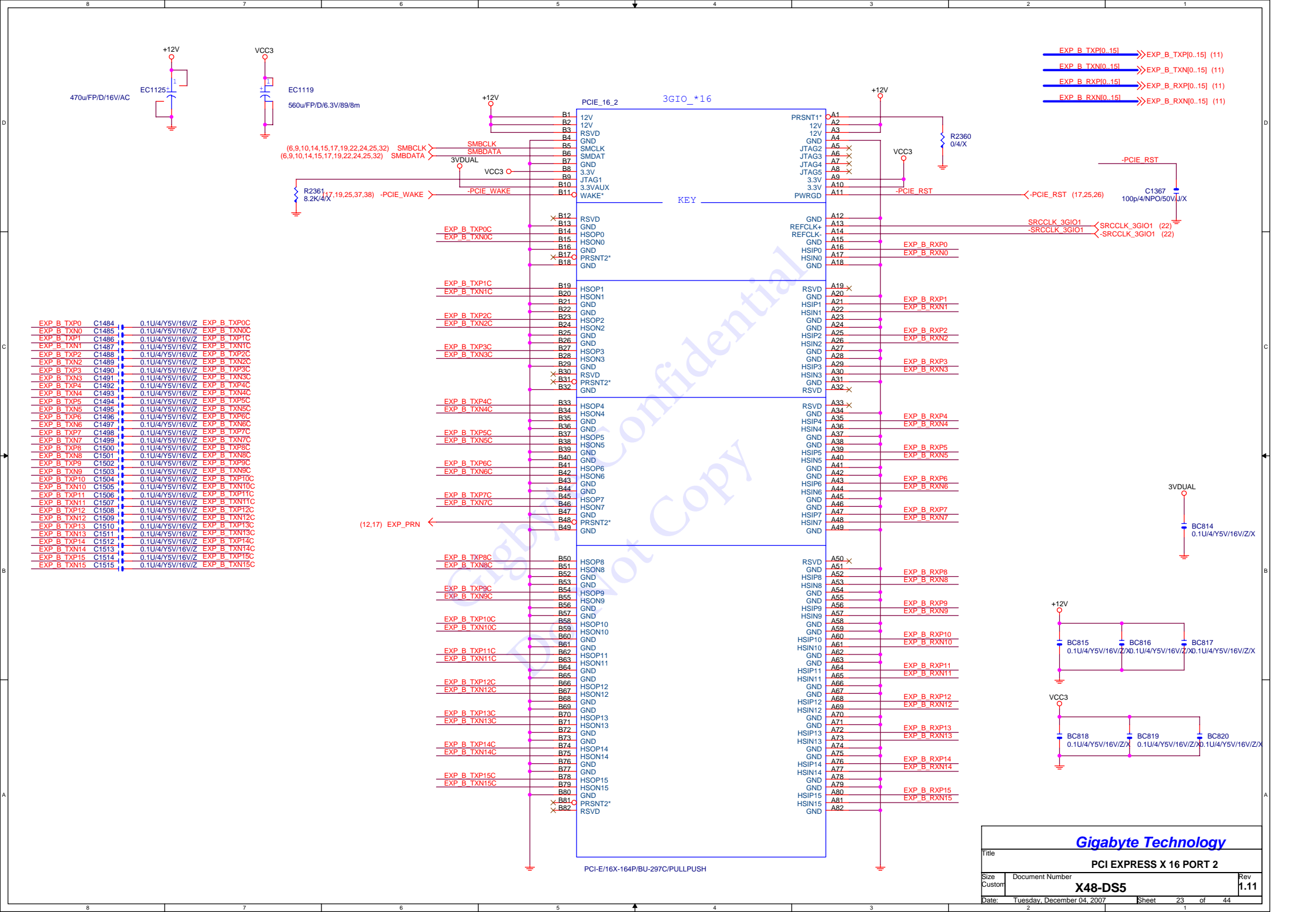




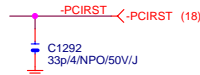
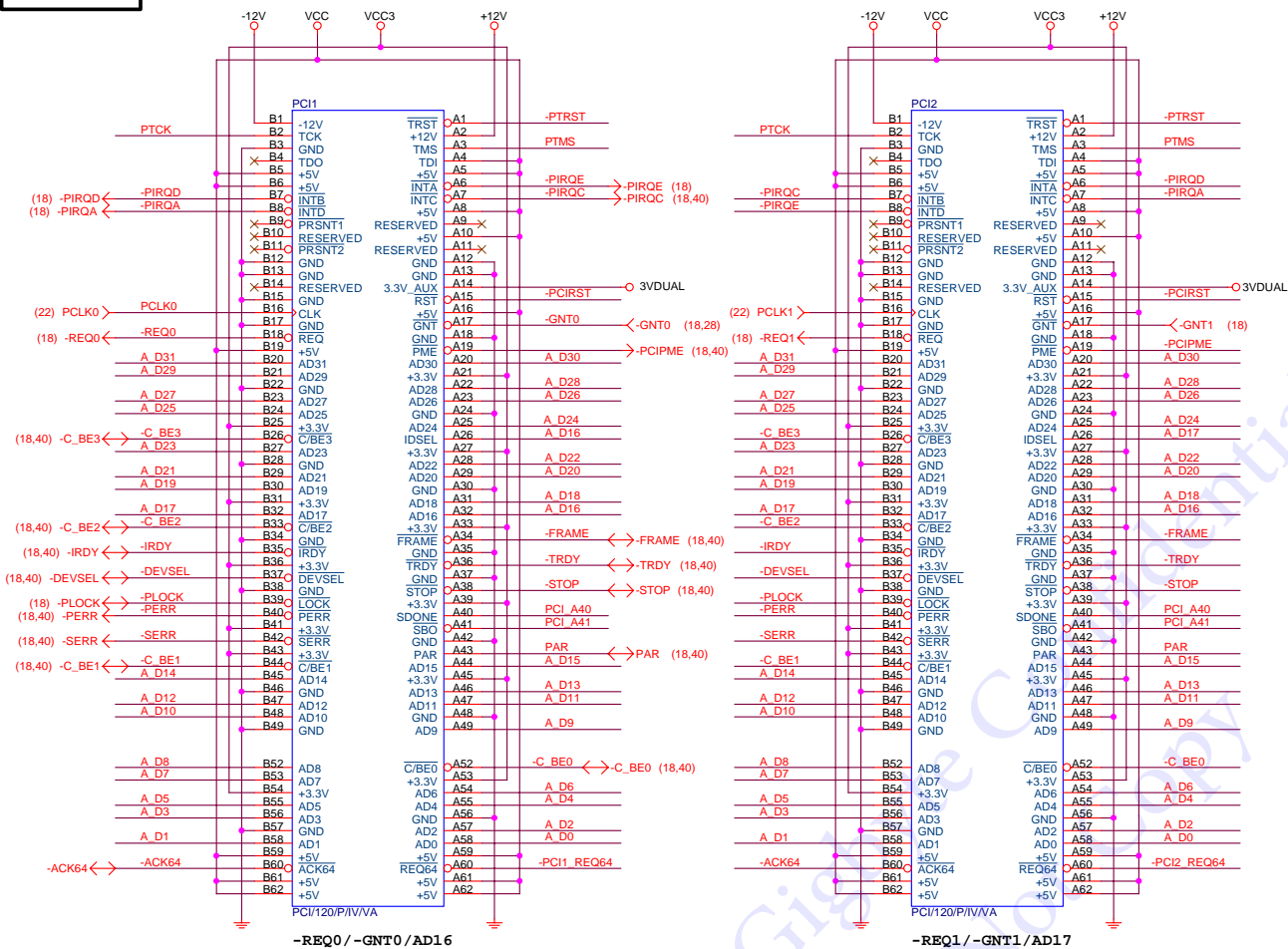


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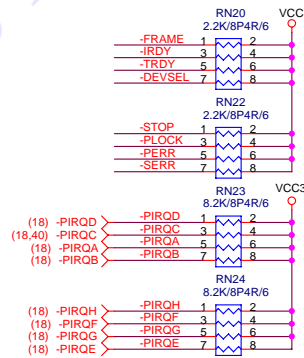
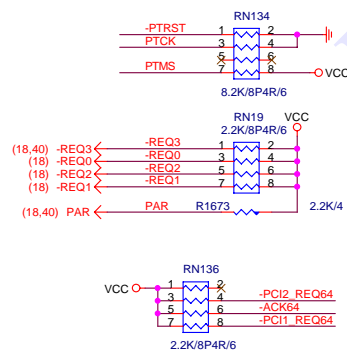
Title			CK505 CLK GEN
Size			X48-DS5
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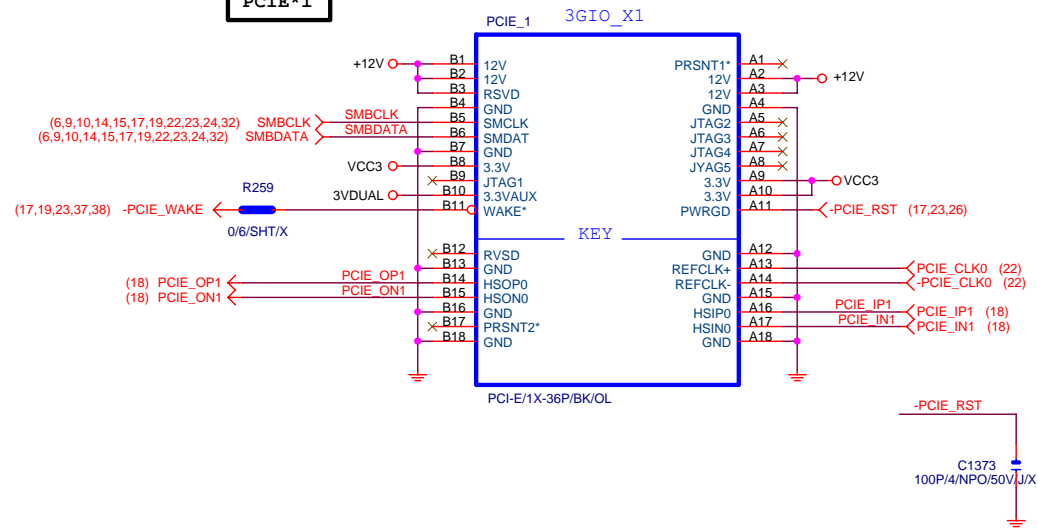
PCI1,2 SLOT



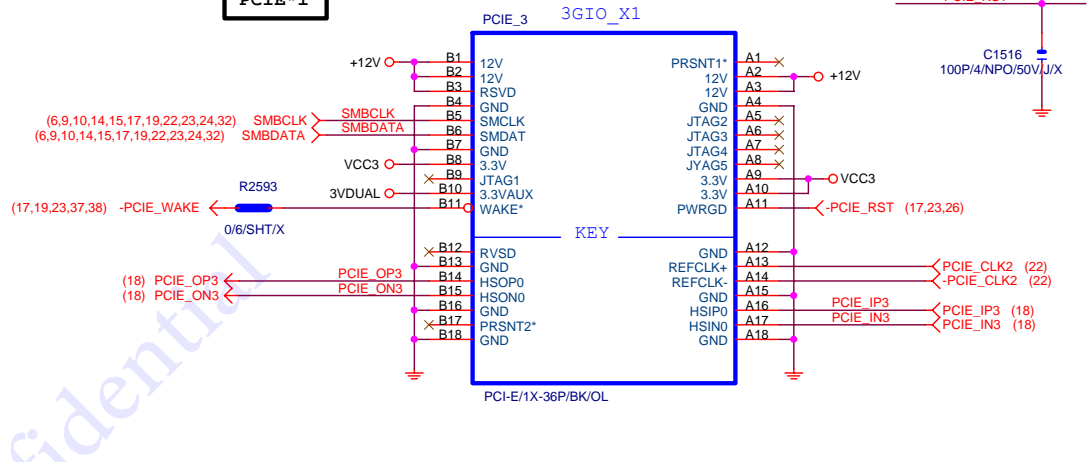
Place close to PCI1



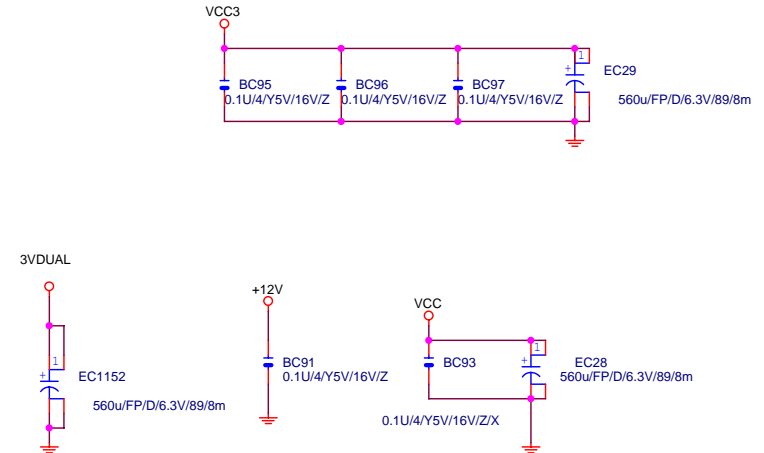
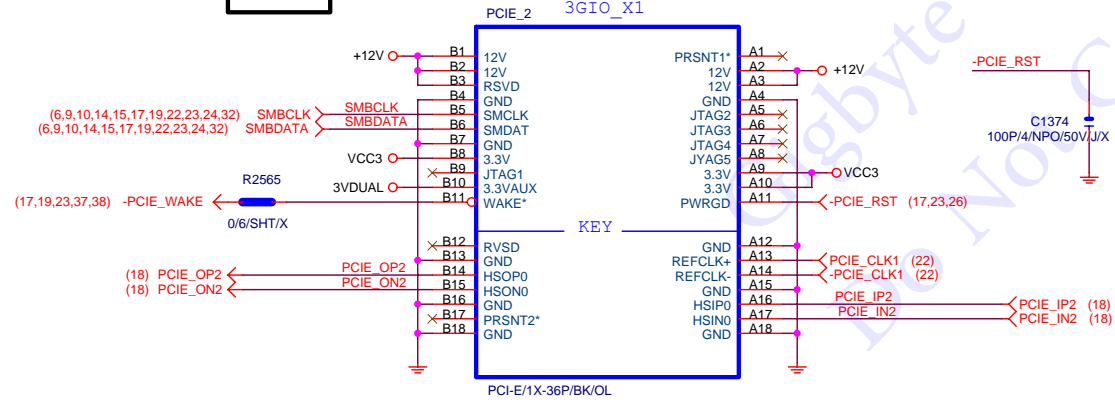
PCIE*1



PCIE*1



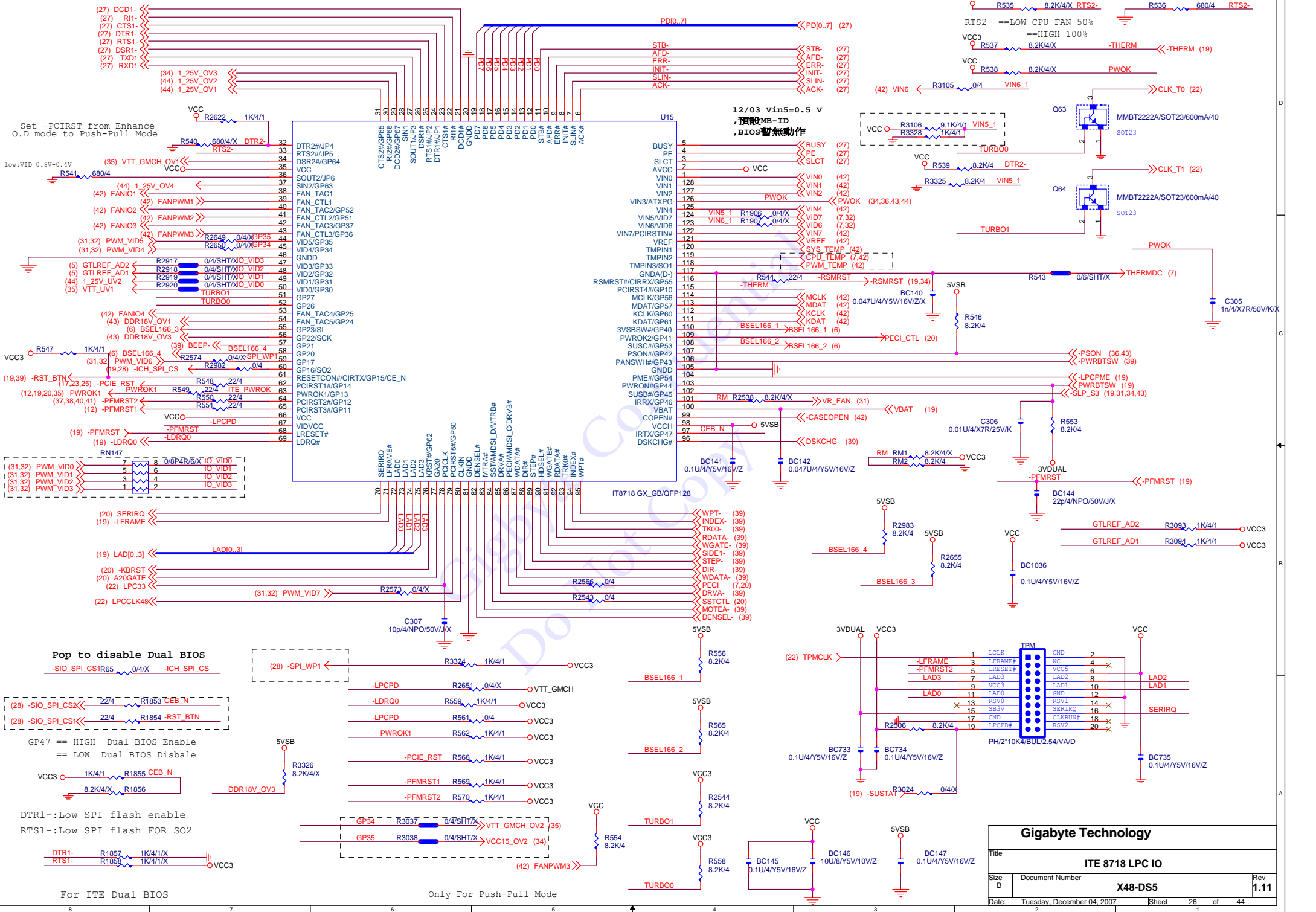
PCIE*1



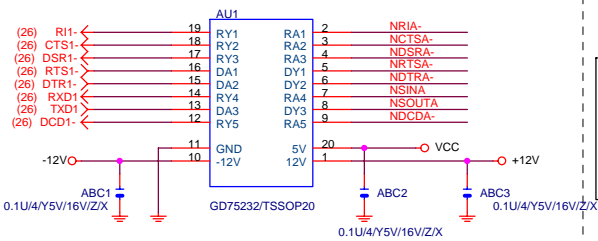
Gigabyte Technology

Title			PCIE_X1 1,2,3 /PCIE SW
Size	Document Number	Rev	
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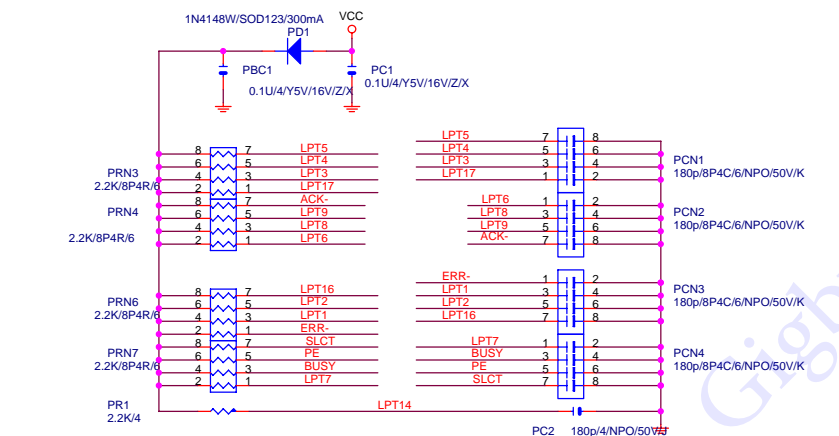
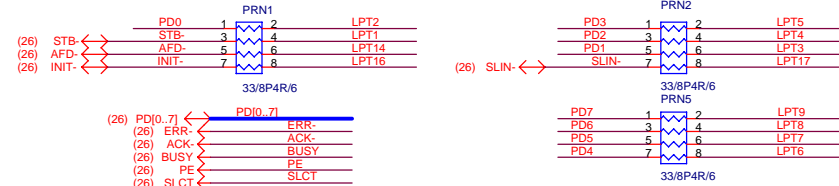
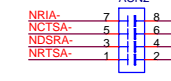
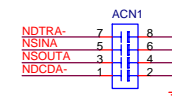
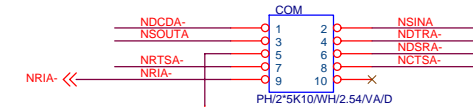
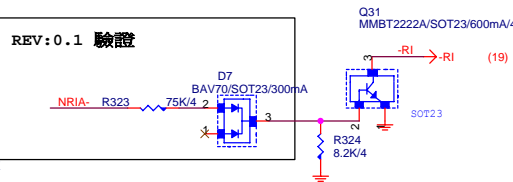


COMA

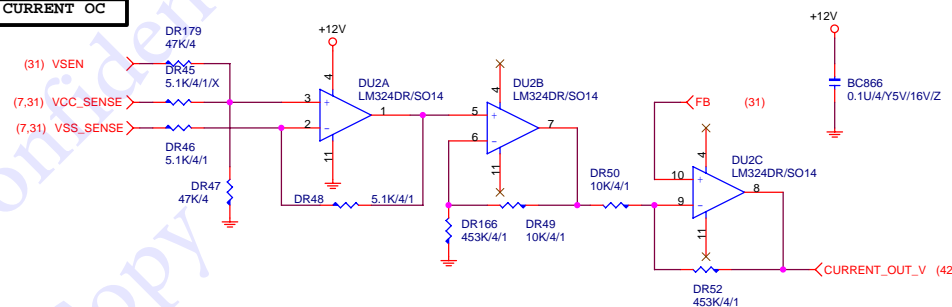


COM RI

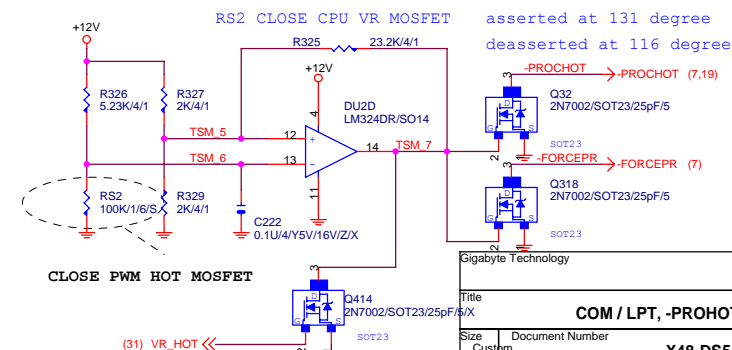
REV:0.1 驗證



DYNAMIC CURRENT OC

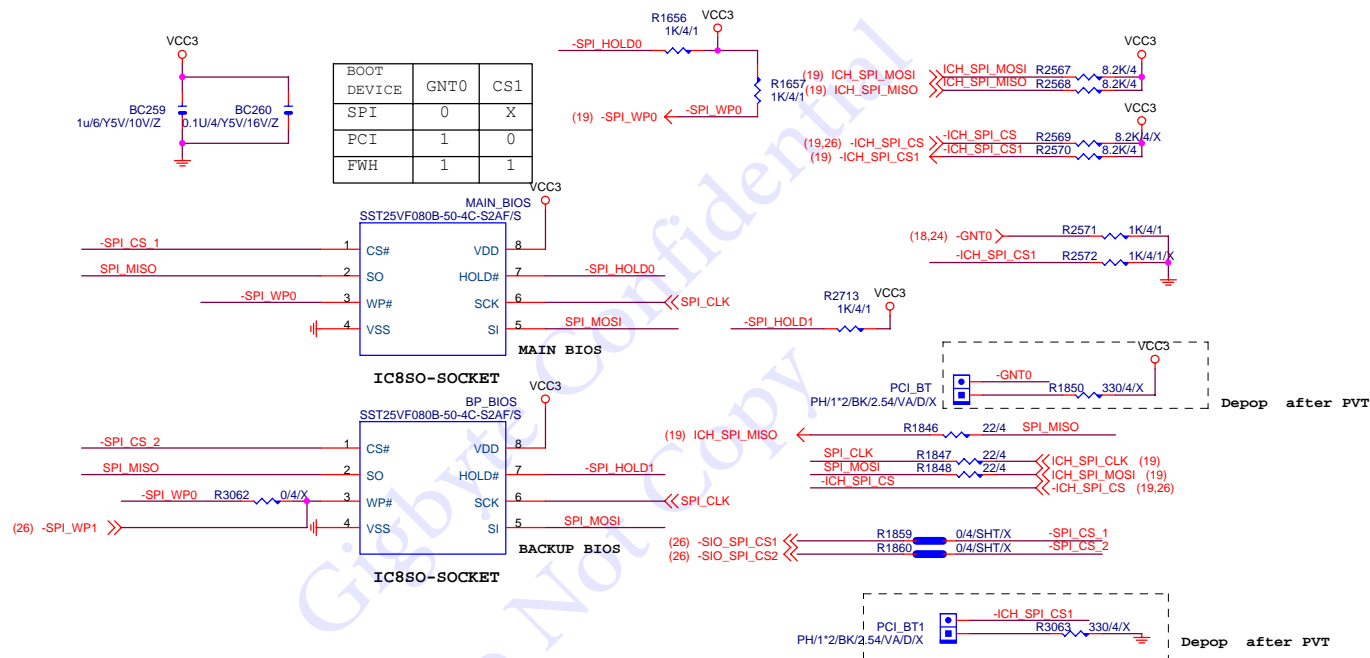
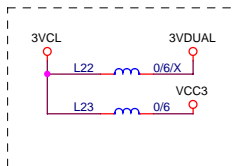


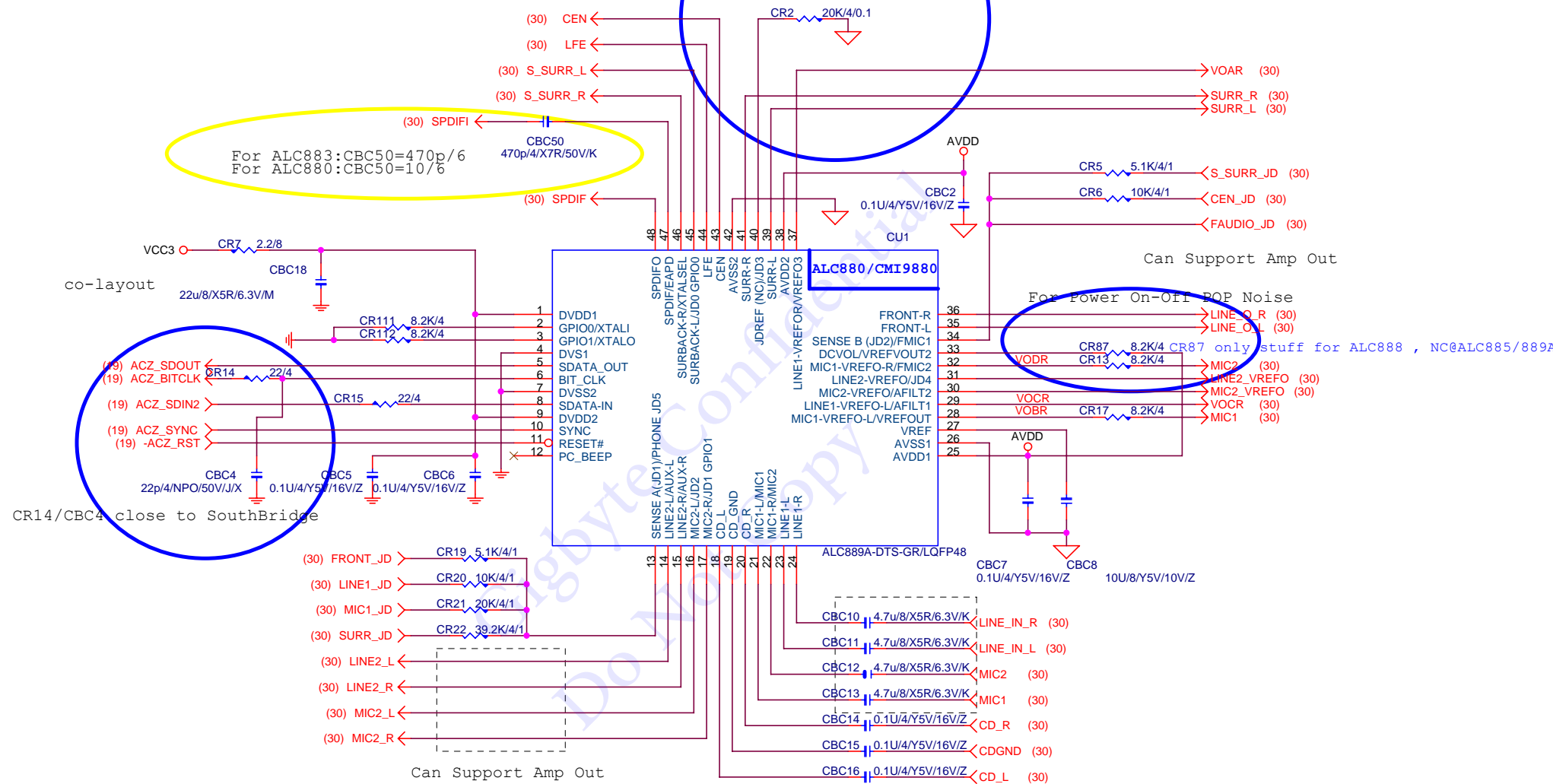
-PROHOT



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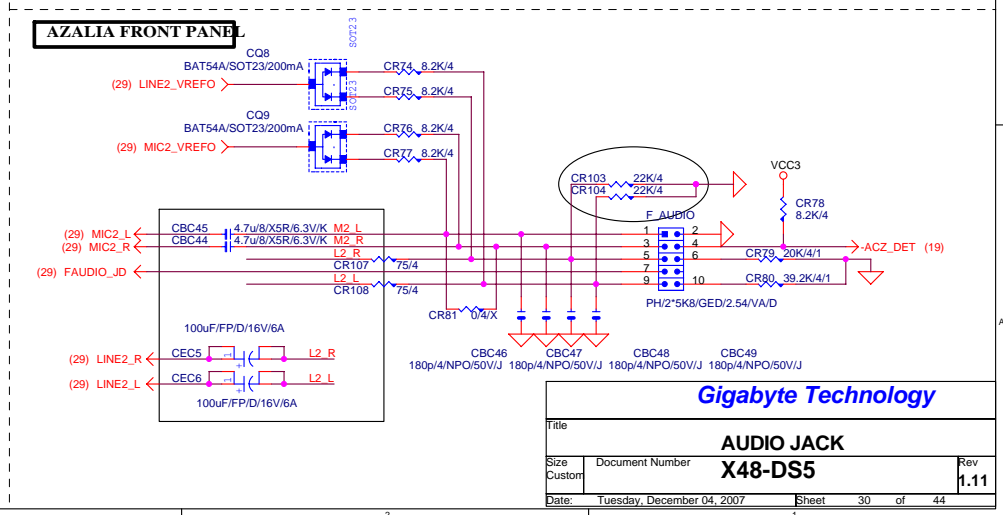
Title			
COM / LPT, -PROHOT,DYNAMIC OC			
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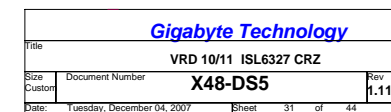


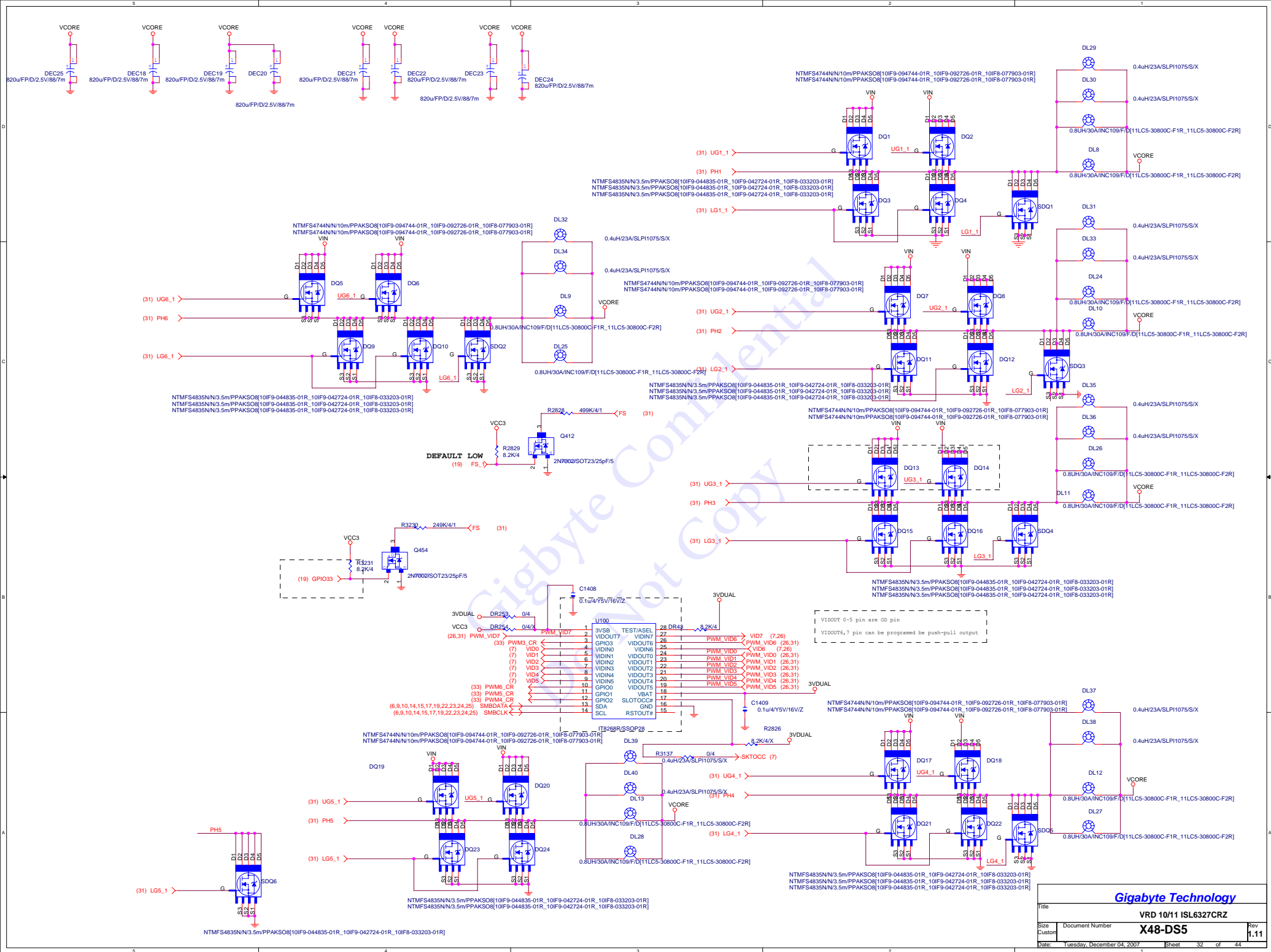


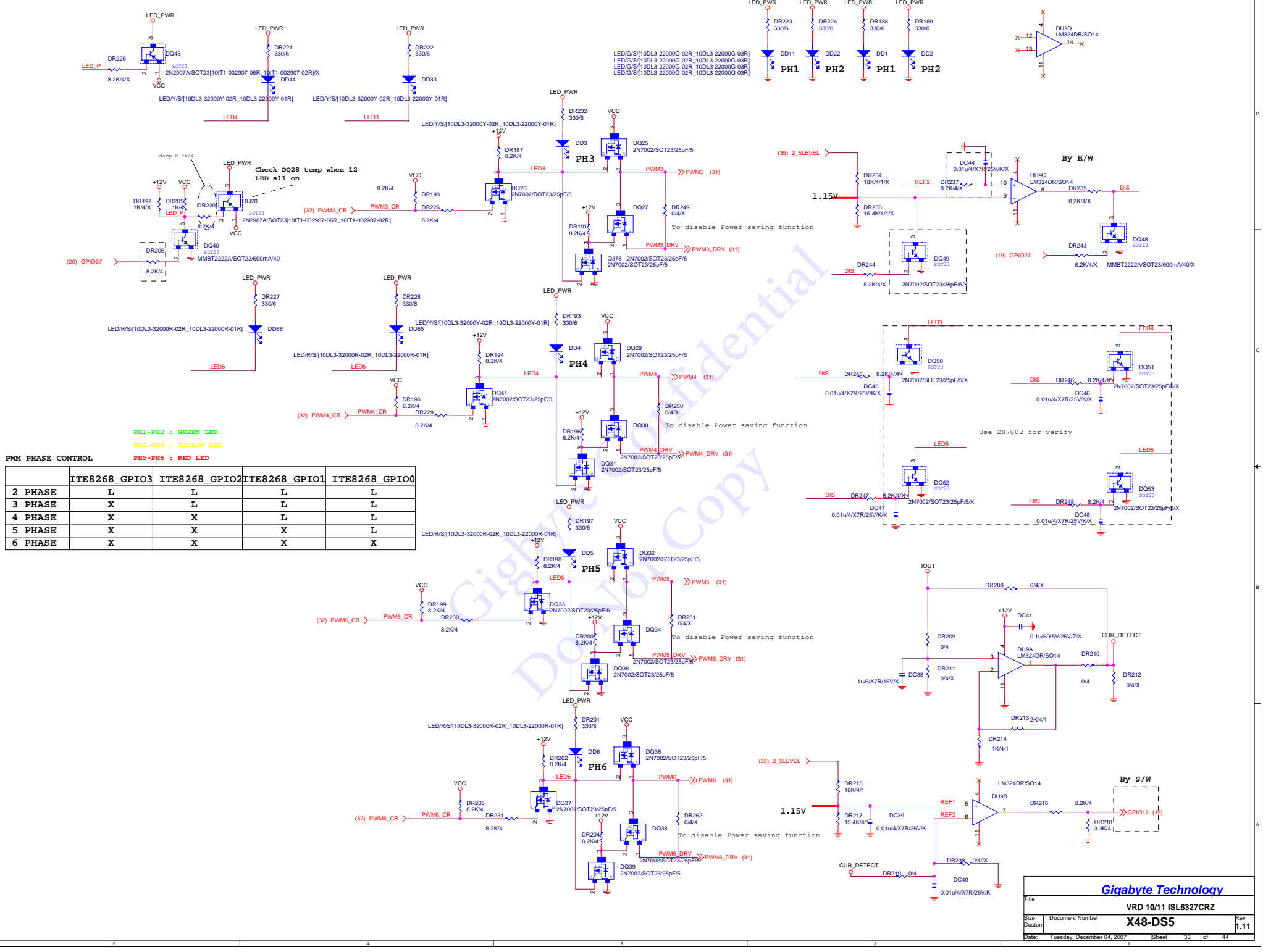
Gigabyte Technology

Title			
HD AUDIO ALC889A			
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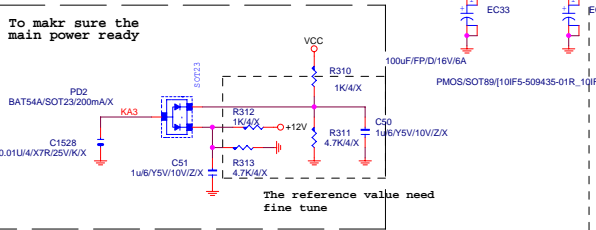
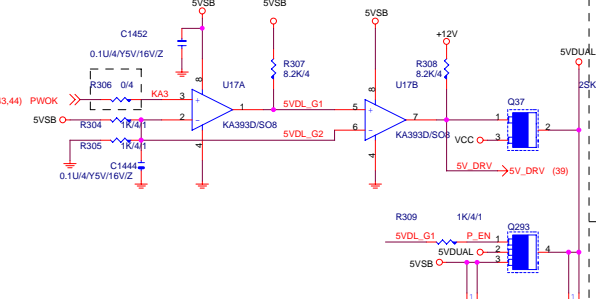


PWM PHASE CONTROL

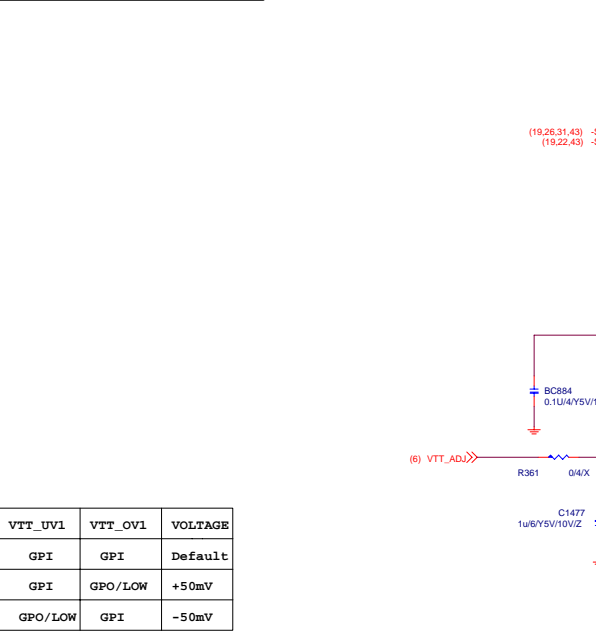
	ITE8268_GPIO3	ITE8268_GPIO2	ITE8268_GPIO1	ITE8268_GPIO0
2 PHASE	L	L	L	L
3 PHASE	X	L	L	L
4 PHASE	X	X	L	L
5 PHASE	X	X	X	L
6 PHASE	X	X	X	X

PH1-PH2 : GREEN LED
PH3-PH4 : YELLOW LED
PH5-PH6 : RED LED

5VDUAL

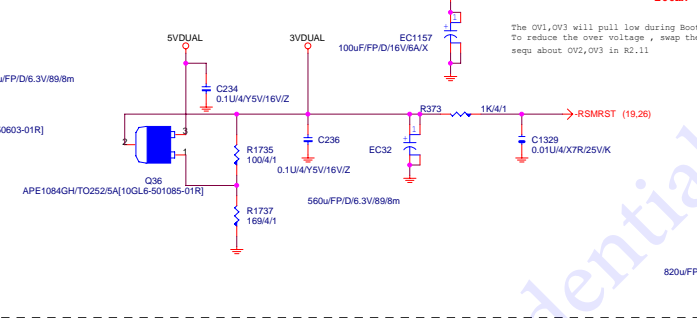


DDR18V/DDRVT/VCC1_05/VTT_GMCH

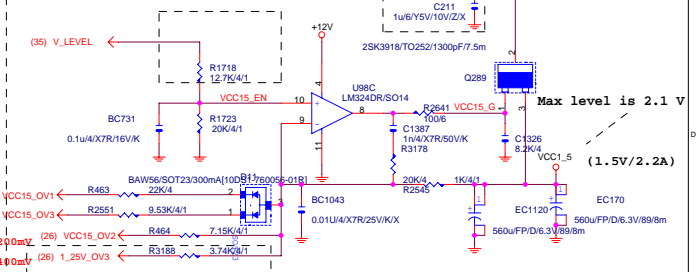


VTT_UV1	VTT_OV1	VOLTAGE
GPI	GPI	Default
GPI	GPO/LOW	+50mV
GPO/LOW	GPI	-50mV

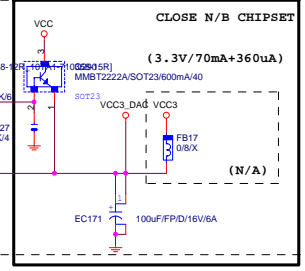
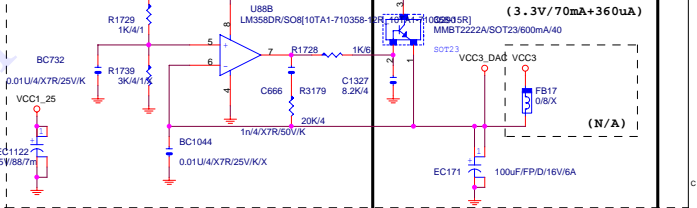
3VDUAL



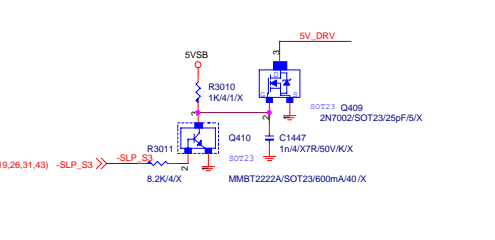
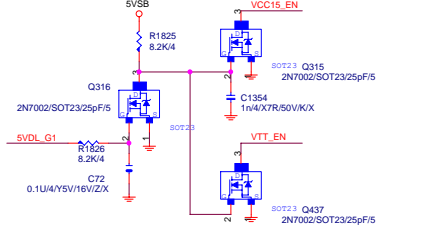
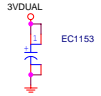
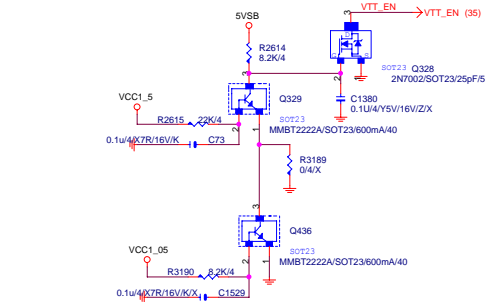
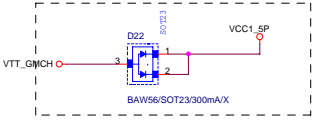
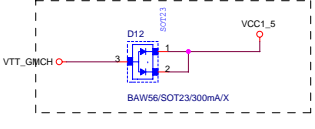
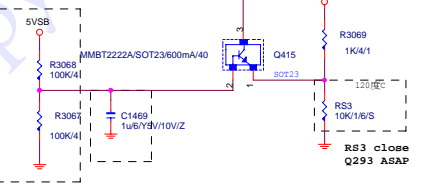
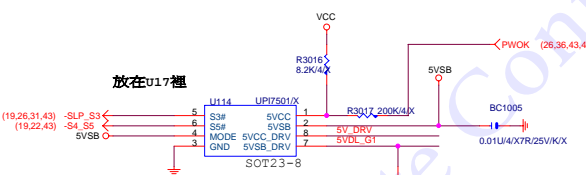
VCC1_5

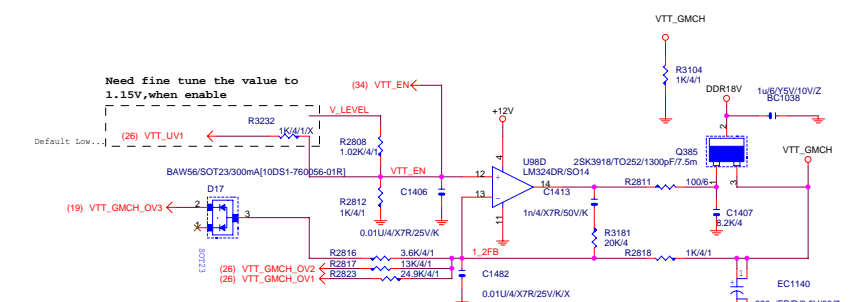
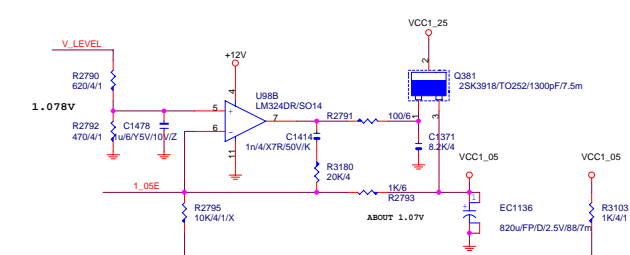
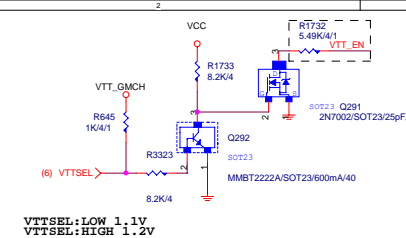


VCC3_DAC

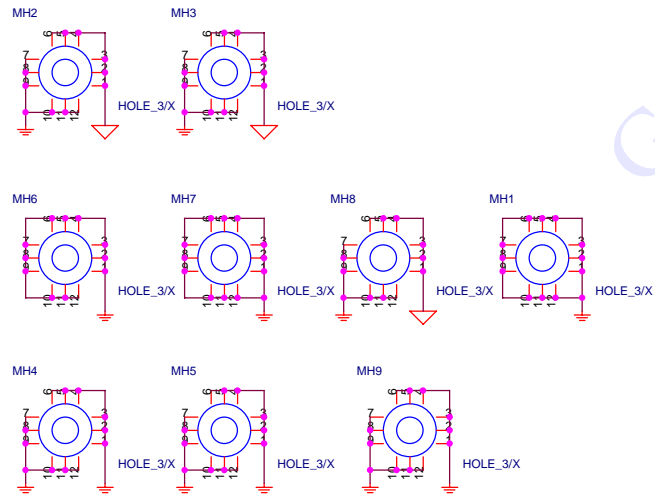
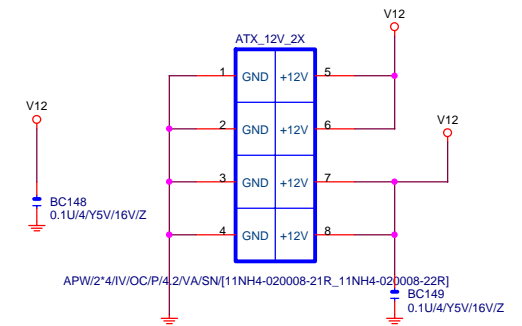
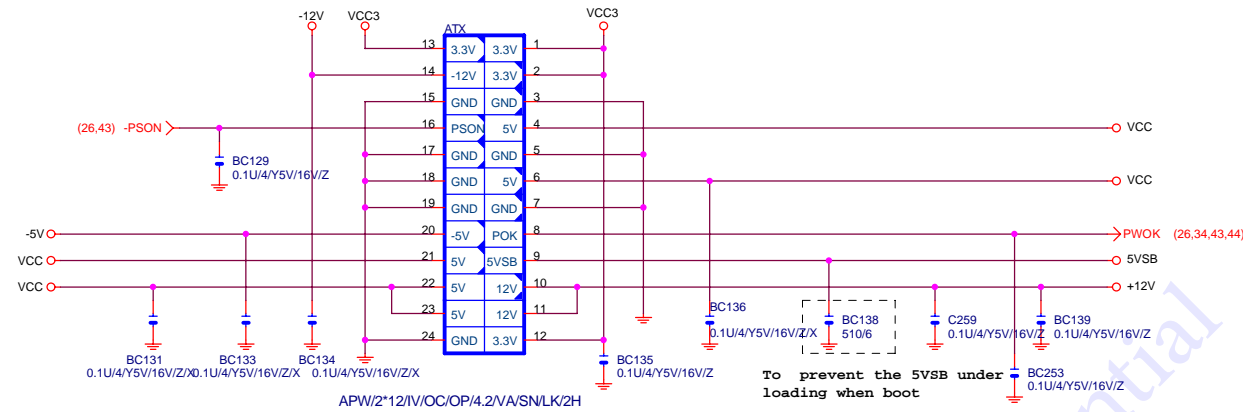


放在U17裡





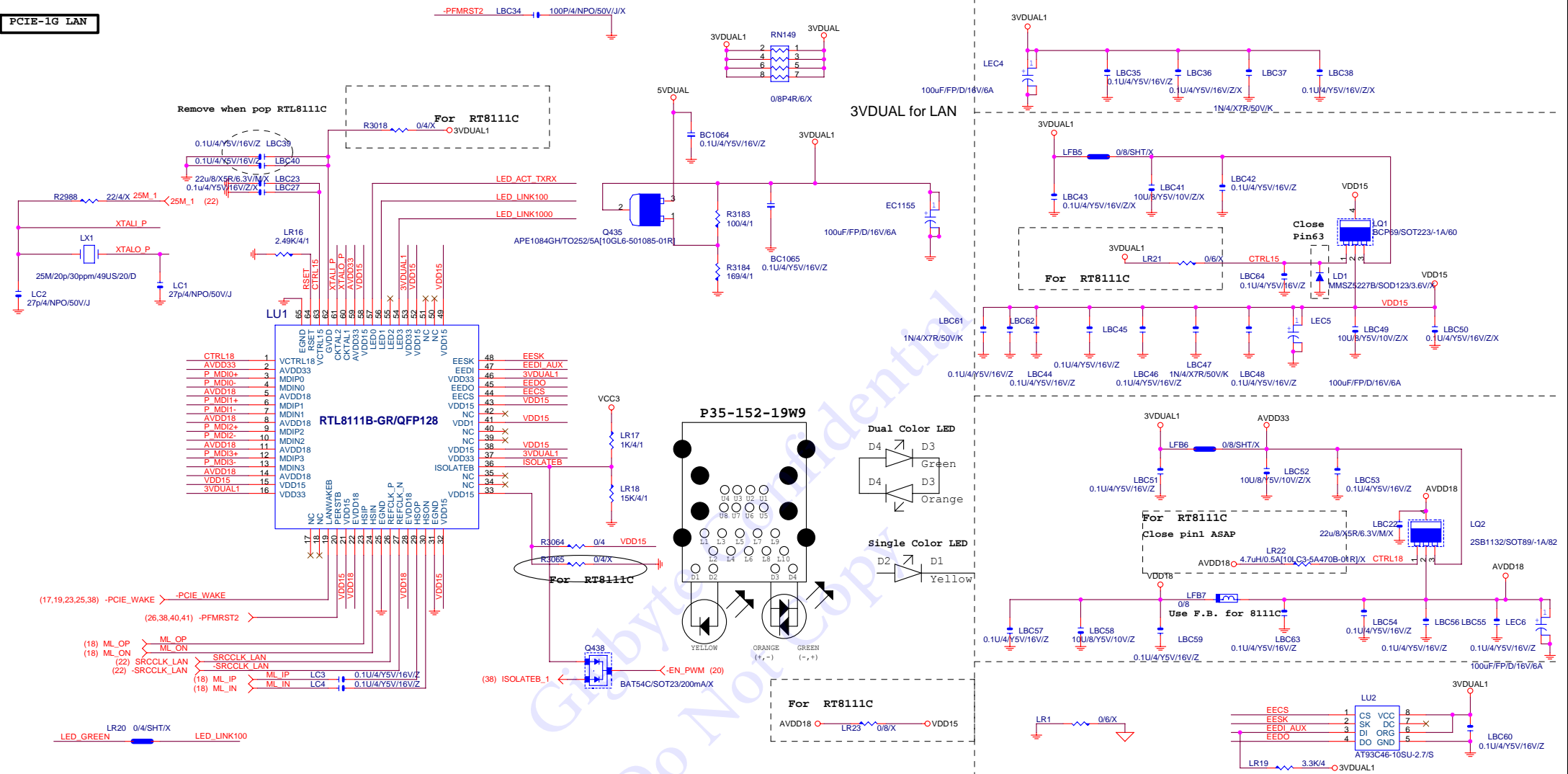
ATX POWER CONNECTOR



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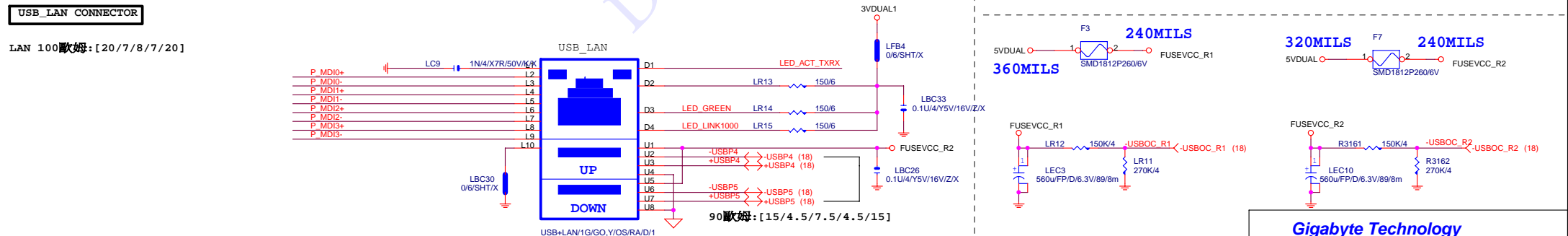
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ATX POWER CONNECTOR		
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PCIE-1G LAN

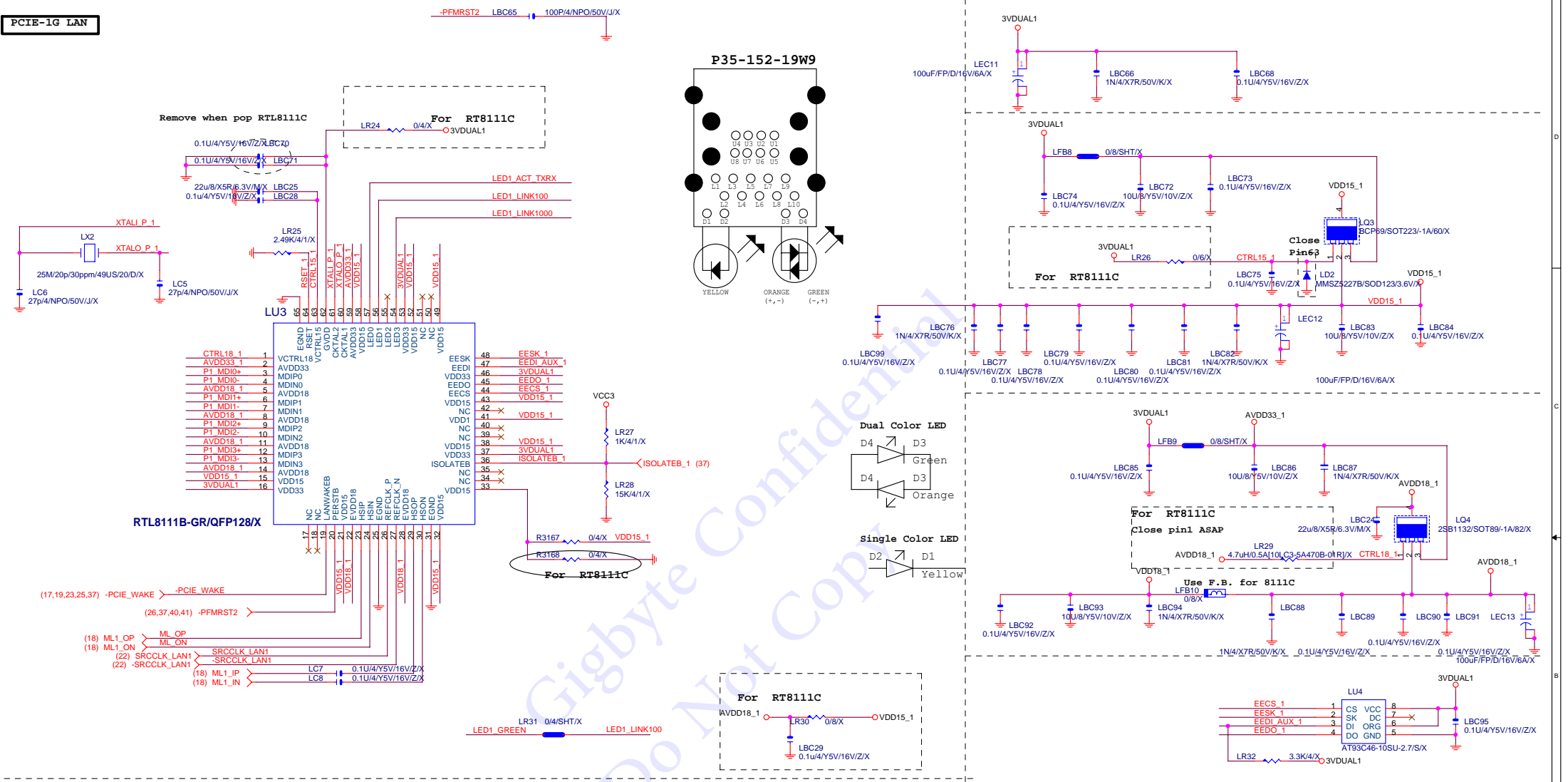


USB_LAN CONNECTOR

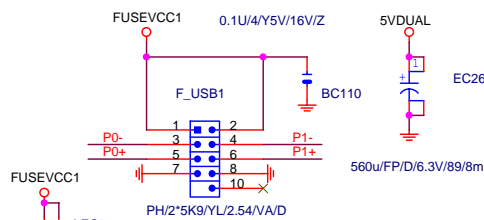
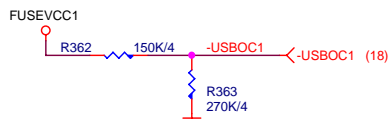
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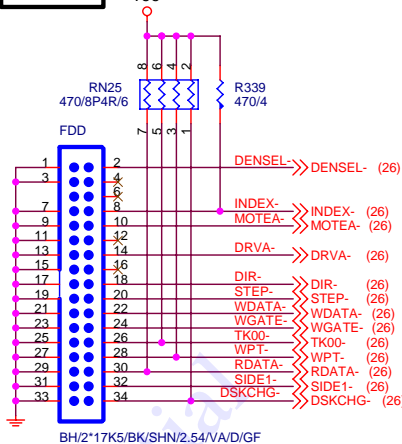
PCIE-1G LAN



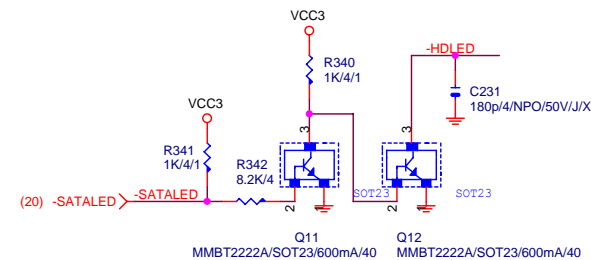
FRONT USB1



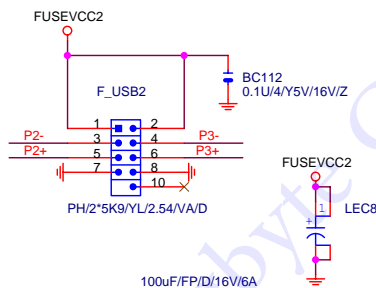
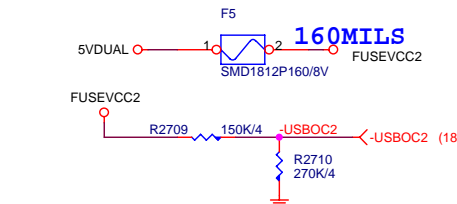
FLOPPY



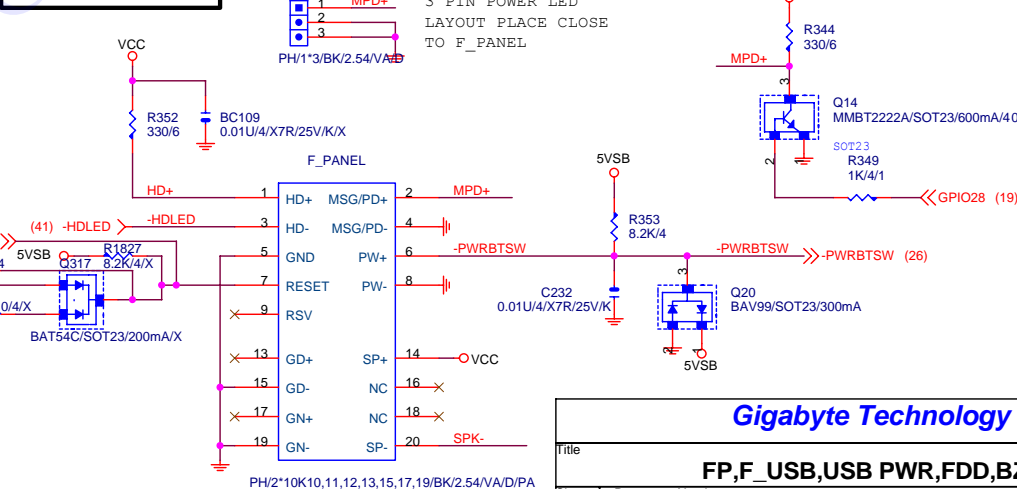
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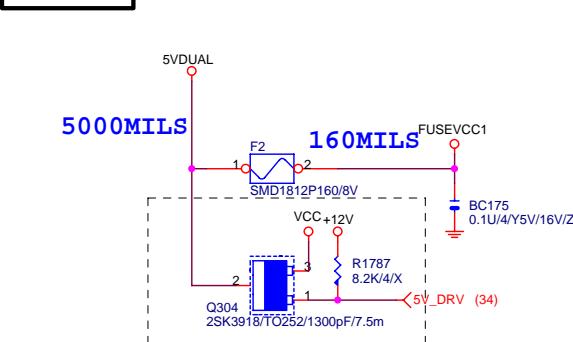
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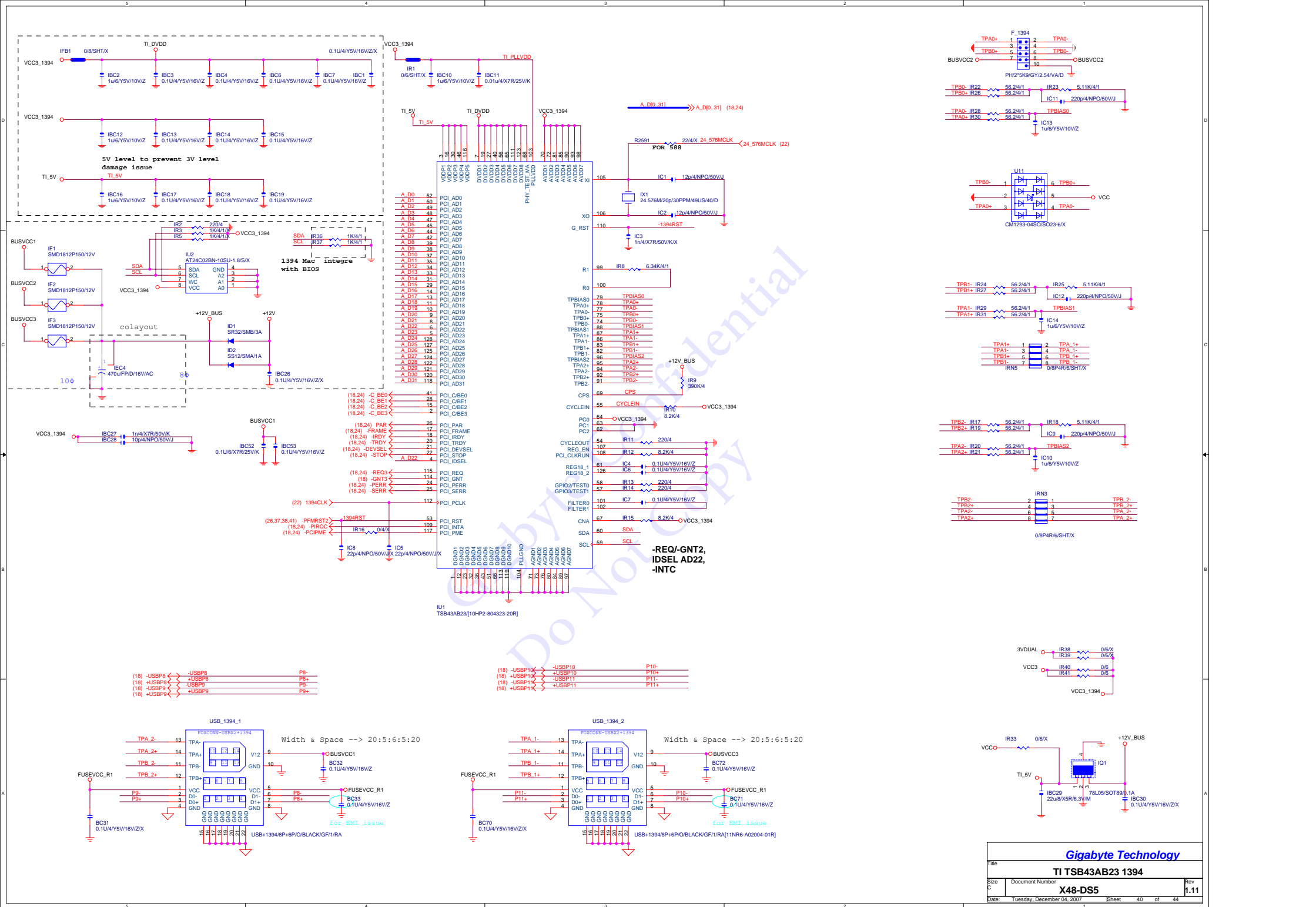
INTEL FRONT PANEL



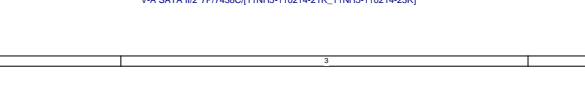
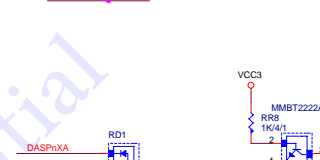
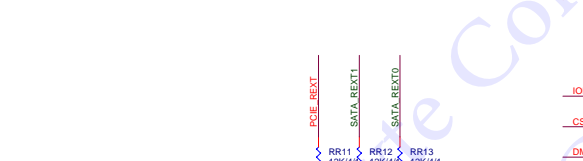
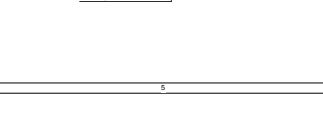
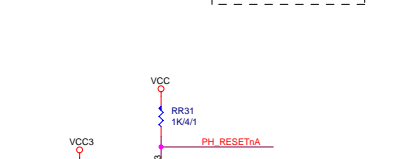
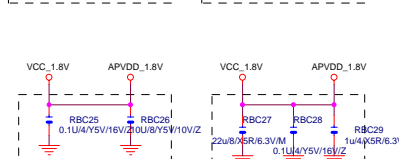
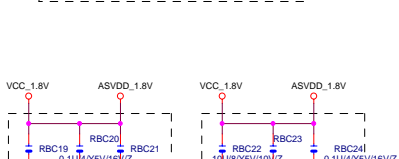
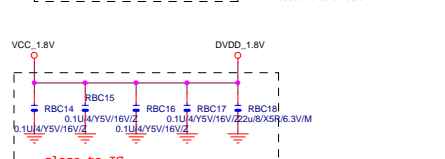
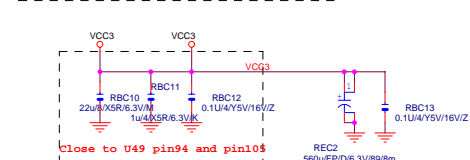
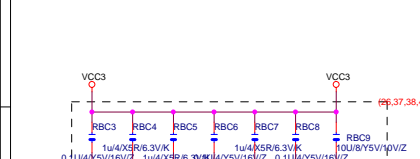
USB POWER



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FP,F_USB,USB PWR,FDD,BZ			
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AMC1117SK/SOT223/0.8A[10GL3-081117-06R]



(26) VREF ←

(26) SYS_TEMP ←

(6) PWM_TEMP ←

(6) CPU_TEMP ←

C1294
1uF/Y5V/10V/Z

C1295
1uF/Y5V/10V/Z

RS1
10K/1/6/S

R1652
30K/6/1

C1296
5.6nF/X7R/25V/K

R1651
10K/4/1

R269
10K/4/1

R270
30K/4/1/X

Case Open Circuits

The schematic diagram illustrates the power supply section of the AD9234 evaluation board. It shows the connection of various power pins (VIN0-VIN4) to the board's power rails (VCORE, DDR18V, VCC3, +12V) through resistors (R366-R377) and capacitors (SC24-SC27, C1476). A current detector (CUR_DET) is also shown.

- VCORE:** Connected to VIN0 through resistor R366 (8.2K/4) and capacitor SC24 (1/4/X7R/25V/K).
- DDR18V:** Connected to VIN1 through resistor R367 (8.2K/4) and capacitor SC25 (0.01u/4/X7R/25V/K).
- VCC3:** Connected to VIN2 through resistor R368 (8.2K/4) and capacitor SC26 (0.1u/4/X7R/25V/K).
- +12V:** Connected to VIN3 through resistor R369 (24K/4/1) and capacitor SC27 (0.01u/4/X7R/25V/K).
- VIN4:** Connected to the +12V rail through resistor R2576 (8.2K/4).
- VIN6:** Connected to the +12V rail through resistor R377 (10K/4/1/X).
- Current Detector:** CUR_DET is connected to the +12V rail through resistor R370 (10K/4/1) and to the current detector pin through resistor R2922 (10K/4/1).
- Capacitor C1476:** A 1u6/Y5V/10V/Z capacitor connected to the +12V rail.

The schematic diagram illustrates the power supply connections for the KB/MS and FUSEVCC_R3 components. The KB/MS component is connected to the SEVCC_R3 and FUSEVCC_R3 power supplies. The FUSEVCC_R3 component is connected to the 5VDUAL power supply. The diagram includes labels for various pins and components, such as KB/MS, SEVCC_R3, FUSEVCC_R3, 5VDUAL, and SMD1812P160/8V.

[illegible]

PWR_FAN
FAN/1*3/WH/A3/2.54/VA/D/SN
SYS FAN
(27)

Figure 10: Linear SYS_FAN

The schematic diagram illustrates the Linear SYS_FAN circuit. It features an LM358 op-amp configured as a voltage follower. The non-inverting input (pin 3) is connected to a voltage divider consisting of R2498 (8.2K/4) and R2499 (1K/4) connected to VCC3, and R2496 (0/4) and R2603 (0/4S/X) connected to ICH_FAN_PWM1 (26). The inverting input (pin 2) is connected to the output (pin 1) and a feedback network consisting of R2497 (47K/4) and R2600 (0/4S/X). The output (pin 1) is connected to the SYS_FAN2 FAN1 pin. The op-amp is powered by +12V and ground. A 100uF/FP/D/16V/6A capacitor is connected to the +12V supply. The circuit also includes a 10T1A-710358-15R relay and a 0344 component. The output of the relay is connected to the SYS_FAN2 FAN1 pin. The circuit is labeled 'Linear SYS_FAN'.

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HWM,KB/MS, FAN CTRL				
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